ADDITIVE MANUFACTURING SOLUTIONS FOR APPLICATION-SPECIFIC MILLIMETER-WAVE WIRELESS SYSTEM DESIGN AND PACKAGING

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ADDITIVE MANUFACTURING SOLUTIONS FOR APPLICATION-SPECIFIC MILLIMETER-WAVE WIRELESS SYSTEM DESIGN AND PACKAGING

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To my father, mother, and sister

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SUMMARY

The ubiquity of wireless technology continues to find new avenues of integration within the vast array of electronic devices used throughout modern society. From over-the-air radio broadcasts stretching across landscapes to real-time collision avoidance sensors in automobiles, the generation and manipulation of electromagnetic radiation has become a indispensable hallmark of engineering ingenuity. In recent decades, the desire for higher data throughput in mobile networking and increased resolution in remote sensing capabilities has pushed for the commercialization of millimeter-wave (mm-Wave) technology, where wireless systems utilize operational frequencies in the range of tens of GHz, an order of magnitude greater than traditional industry solutions. This increase in frequency enables wider operational bandwidths while presenting its fair share of challenges for the modern RF engineer. The resulting reduction in wavelength requires additional attention to system packaging and integration schemes to reduce detrimental parasitic losses and achieve high system efficiency, as common circuit structures become more electromagnetically significant within the mm-Wave regime.

In order to address these challenges, novel integration schemes such as system-on-chip (SoC) and system-in-package (SiP) have garnered attention as enabling technologies, where essential system-level components are integrated into a single chip (SoC) or package (SiP). These methods reduce assembly overhead and losses between components while simultaneously promoting system miniaturization, facilitating adoption into the small form factors of modern wireless devices. With the adoption of SiP technology with wireless systems, efforts are also pushing towards the integration of antennas within microelectronic packages to further reduce interconnection losses and improve the crucial link between a wireless device's first point-of-contact, the antenna, and the front end of an RF module.

Recent efforts have demonstrated additive manufacturing (AM) fabrication techniques as an effective, low-cost tooling medium for the development and assembly of electronic

devices. The vertically-integrated nature of AM, where a variety of electronic materials are patterned in an on-demand, layer-by-layer fashion, proves to be an enabling technology for the realization of next-generation wireless systems. As the materials and processes of such technologies as inkjet and 3D printing continue to mature and grow in capabilities, AM is increasingly establishing its presence with the fields of microelectronic packaging and wireless system integration as a robust and enabling tooling methodology.

This thesis outlines the convergence of AM technology with the development of SiP integration schemes for mm-Wave wireless systems. First-of-their-kind demonstrations of fundamental system and package components, such as high gain antennas, interconnects, and "smart" chip encapsulants, are presented utilizing fully-additive printing methods. The technologies outlined in these efforts highlight the potential for AM to further increase the design flexibility of mm-Wave systems at the module and device level, offering a new precedent of rapid, application-specific reconfigurability for the next generation of wireless technology.

CHAPTER 1
INTRODUCTION

Growing trends in emerging wireless technologies are pushing for the realization of high-bandwidth data transmission and miniaturized form factor, along with a necessary reduction in fabrication cost. This next generation of mobile communication systems has highlighted the field of millimeter-wave (mm-Wave) wireless technology, where carrier frequencies operate within the range of tens to hundreds of gigahertz. This increase in frequency from typical commercial microwave technologies allows for wider channel bandwidths, establishing interest in such fields as autonomous automotive radar sensing, vehicle-to-vehicle (V2V) communication, and 5G gigabit wireless networks. Because of the reduction of wavelength throughout the mm-Wave regime, packaging technology becomes especially important in the development of any practical wireless system. In order to miniaturize systems and reduce destructive high-frequency parasitics, the realization of system-in-package (SiP) packaging solutions is an area of gowing interest, where integrated circuit (IC) dies can be integrated directly with peripheral circuit components, such as other ICs, antennas, and various other passive components required in any modern wireless system.

In a typical mm-Wave SiP architecture, monolithic microwave integrated circuit (MMIC) dies are integrated with accompanying system components into a single module, where careful attention is placed on the design of routing circuitry, interconnects, and encapsulants to seal sensitive electronics from an operating environment. Three-dimensional (3D) first-level interconnects are required to interface a MMIC die with a packaging substrate and other electronic components within the same package. The two most common methods of realizing these interconnections are wire/ribbon bonding and flip-chip techniques. Wire bonding is a relatively cheap and rapid interconnection option, yet it is often prone to sway upon encapsulant molding and high parasitic inductance, often requiring external

or on-chip passive components for compensation at mm-wave frequencies [1]. Flip-chip techniques reduce interconnection length and parasitics yet suffer from high sensitivity to coefficient of thermal expansion (CTE) mismatch as well as circuit detuning from the close proximity to on-package signal routing below the bumped IC [2]. The development of robust low-loss first-level interconnects in the mm-Wave regime is an area of continued research with a direct impact on the efficiency of a wireless system, where low cost, high yield, and rapid tooling are highlighted goals with respect to manufacturing.

Recent efforts in the development of advanced electronic fabrication methods have highlighted the effectiveness of additive manufacturing technologies for wireless systems. Additive manufacturing enables the precise on-demand patterning of functional materials with reduced waste and tooling costs compared to standard subtractive lithography-based methods. Inkjet and 3D printing technologies allow for the selective deposition of electronic materials in a 3D fashion, where dielectric and metallic patterns can be fabricated directly onto virtually any host to create fully-printed, vertically-integrated electronic systems and packages [3, 4, 5]. Specifically from a wireless perspective, inkjet printing offers the advantage of incorporating printed interconnects and multilayer antenna structures with wireless dies and packages in an efficient SiP scenario, where conformal fully-printed interconnection and on-demand antenna patterning techniques reduce losses between SiP components and improve matching throughout [6, 7, 8]. Additionally, the continued study of the materials and processes behind 3D printing techniques allows for the integration and innovation of advanced fabrication methods to enhance emerging wireless system designs specifically within the mm-wave regime [9, 10, 11]. The implementation of these additive 3D manufacturing technologies enable the design of highly functional "smart" wireless packages, breaking from the mold of traditional SiP architectures and introducing a new paradigm in the field of advanced microelectronic packaging.

1.1 Research Objectives

The objective of this research is to explore the development, characterization, and implementation of hybrid inkjet and 3D printing processes to provide fundamental solutions to the growing field of wireless mm-Wave packaging. Specifically, this thesis focuses on the following:

1. The development and characterization of multilayer, multi-material inkjet printing processes to realize on-demand high-gain mm-Wave antenna integration in a SiP fashion

2. The design and fist-of-its-kind implementation of fully-printed first-level interconnects for mm-Wave MMIC dies, along with an apples-to-apples comparison with traditional solutions

3. The realization of novel printed "smart" packaging through a hybrid inkjet-3D printing approach, with demonstrations of encapsulant-integrated mm-Wave vias, microfluidic networks, and shielding structures reaching for the first time into the THz regime

1.2 Thesis Outline

This thesis is organized as follows:

1. Chapter 2 presents a review of inkjet and 3D printing processes and materials

2. Chapter 3 presents a review of mm-Wave SiP antenna integration and interconnection techniques through means of traditional and additive manufacturing procedures

3. Chapter 4 presents the additive processes involved with developing fully-printed mm-Wave antennas integrated in a SiP fashion

4. Chapter 5 presents the development of fully-printed first-level in surface-mount and cavity-embedded assembly configurations

5. Chapter 6 presents the concept of printed “smart” wireless packages along with fundamental demonstrations of functional package-integrated components

6. Chapter 7 concludes and discusses future efforts

CHAPTER 2

REVIEW OF ADDITIVE MANUFACTURING PROCESSES

Additive material printing offers an alternative approach to the traditional methods of subtractive electronic fabrication. Subtractive lithography-based methods require the use of patterning masks, electronic plating, planar material growth, chemical etchants, and various other procedures to both deposit and remove materials from host substrates. With additive manufacturing, mass material deposition and subsequent removal is replaced with selective, direct patterning, where the only materials used are materials directly constructing the desired electronic patterns and structures.

Through the utilization of conductive and insulating ink/filament materials, direct printing methods such as inkjet and 3D printing are capable of fabricating flexible and rigid multilayer antenna structures in a purely additive process [12, 13]. The entire stack-up of a multilayer circuit board, including conductive metallization and thick dielectric substrates, can be achieved with inkjet printing, removing the need for multi-laminate processing, trimming, and bonding while allowing for integration with system-level RF components as a post-processing fabrication method. 3D printing further extends the versatility of printed systems into an unlimited variety of applications, where flexible plastics and conductors can be used to realize wearable, reconfigurable wireless systems with a feasibly lowered cost and improved functionality.

2.1 Inkjet Printing Techniques

Inkjet printing is an additive technology that consists of three general elements: a dispensary apparatus, an ink material, and a host substrate. The dispensary apparatus is typically an ink cartridge consisting of an ink reservoir and a device to eject drops onto a substrate, which is commonly realized through a piezoelectric MEMS device. Ink materials can range

in material composition and functionality, including conductive nanoparticle suspensions and polymeric dielectric solutions. The host substrate accepts and is patterned by the ink droplets ejected from the dispensary apparatus, where certain material characteristics such as surface tension and fluidic wetting must be taken into account in order to ensure accurate material patterning.

The mechanical actuators used within inkjet printing vary in the physical mechanisms used to dispense ink droplets from a dispensary onto a substrate. For modern inkjet printing systems, four main actuators are used:

1. *Thermal* – Ink is heated within a cavity until volume and pressure is increased enough to force a droplet ejection. Very low cost, yet relatively high drop volume (80–100 pL [14].

2. *Piezoelectric* – Ink is pulled into a cavity and then ejected in droplets using a piezoelectrically actuated membrane. Higher control over droplet formation and wide variety of allowable ink materials.

3. *Electrodynamic* – A large electric field is applied between a nozzle and conductive platten below a host substrate, where ink droplets are forcefully ejected from a nozzle. Capable of producing very small drop volumes (< 1 fL), yet require inks to contain free ions [15].

4. *Acoustic* – Ultrasonic waves are focused on an ink meniscus, overcoming surface tension and allowing a droplet to be ejected. Reduced nozzle clogging and increased precision in drop volume variability [16].

2.1.1 Ink Temperature and Jetting Voltage

The effectiveness of an inkjet-printed fabrication begins with ink jetting characteristics. Using a piezoelectric droplet jetting system, the voltage of the piezoelectric actuator helps determine the formulation and expulsion of ink droplets from the cartridge. In operation, a

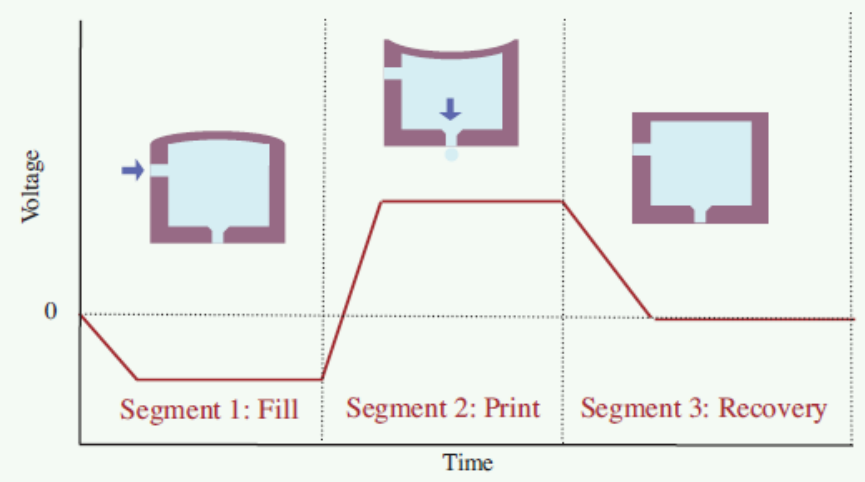


Figure 2.1: General acuator waveform for ink jetting [18].

time dependent voltage waveform is utilized to bring the actuator through stages of intake, drop jetting, and recovery. Figure 2.1 shows a generalized cartridge waveform for ink jetting. The voltages required to expel well-formed droplets from the cartridge relate heavily to the viscosity and temperature of the ink, which are typically in the order of 12–15 cP and 30–40 °C, respectively [17].

2.1.2 Substrate Surface Energy Modification

Once a droplet is expelled from the cartridge, material agreement between the ink and the substrate must be made in order to produce an accurate, repeatable pattern. This agreement is made with the relationship between the surface energy of the substrate and the surface tension and contact angle of the ink. When the surface energy of the substrate is much higher than the surface tension of the ink droplet, the contact angle of the ink will be too small and the ink will spread greatly from its initial drop diameter. In the inverse situation, the contact angle of the ink droplet will be too high and will pull away from the substrate [19]. Figure 2.2 shows a general contact angle measurement of a liquid droplet on a solid substrate that is used to determine the surface energy of a substrate. The variables γ_{SV}, γ_{SL}, and γ_{LV} represent the free energies between solid/vapor, solid/liquid, and liquid/vapor interfaces, respectively. The relationship of these energies with a contact angle

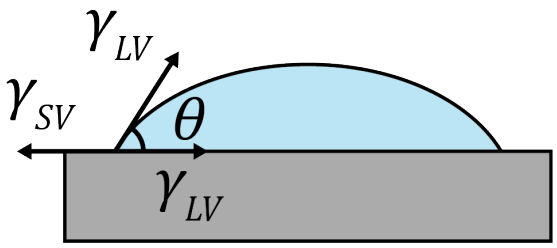


Figure 2.2: Droplet wetting on substrate displaying contact angle θ, used to determine substrate surface energy.

can be simplified and expressed with planar geometry as the Young-Dupre relation, shown in Equation 2.1 [20]:

$$\gamma_{SV} = \gamma_{SL} + \gamma_{LV} \cos\theta \tag{2.1}$$

Generally, good wetting of an ink to a substrate occurs when the surface energy of the substrate is greater than the surface tension of the ink by 10–$20\,\mathrm{mN/m}$. The surface energy of a substrate can be modified through raising the temperature of the substrate or UV ozone surface treatment, which will decrease and increase the surface energy of the substrate, respectively.

2.1.3 Ink Formulations and Characteristics

As previously stated, reliable inkjet printing requires fine-tuned ink formulations consisting of a certain viscosity and surface energy. Multilayer inkjet-printed devices require the use of both high conductivity metallic inks and thick film dielectric inks in order to allow for structural versatility, device miniaturization, and purely selective system deposition.

Conductive Silver Nanoparticle-Based Inks

The most efficient conductive inks used within inkjet printing are metallic in essence but differ in their material composition and processing. Silver nanoparticle (SNP) solutions of noble metals, such as silver and gold, currently dominate the market of commercially

available metallic conducting inks. These inks are composed of a suspension of metallic nanoparticles within an alcoholic solvent solution. Upon printing, the solvent materials are evaporated with a low temperature thermal treatment and then sintered with either thermal baking or laser rastering, offering a method of metallic patterning that does not interfere with low-temperature substrates, such as polymeric or fibrous materials [17]. These methods of deposition and curing have demonstrated conductivity in the order of $10^7\,\mathrm{S/m}$, $5\times$ less than that of bulk silver, with a layer thickness of approximately 0.5–$1\,\mu\mathrm{m}$ per layer. Non-noble metals, such as copper, are difficult to process as nanoparticles because of their high oxidation rates during sintering. As an alternative, metallic catalyst inks can be used to pattern a latent image of a conductive topology, followed by the electroless chemical plating of metal onto the printed pattern [21].

Three varieties of SNP inks are utilized for the efforts presented in this thesis, summarized in Table 2.1. All three inks are relatively similar in printing conditions and composition, where wetting characteristics and commercial availability are the main factors for ink selection. Sintering temperature and duration are typically selected based on the thermal characteristics of the host substrate, which range from 120–$200\,^\circ\mathrm{C}$ and 0.5–$2\,\mathrm{h}$, respectively.

Table 2.1: Summary of Highlighted Silver Nanoparticle (SNP) Inks

Manufacturer	Ink Model	Solvent	Ag Content	Vol. Resistivity
Cabot	CCI-300	Ethanol	20 wt%	$10\,\mu\Omega\,\mathrm{cm}$
ANP	Silverjet DGP-40LT-15C	TGME	30-35 wt%	$11\,\mu\Omega\,\mathrm{cm}$
Sun Chemical	SunTronic EMD5730	Ethanediol	40 wt%	5–$30\,\mu\Omega\,\mathrm{cm}$

Thick Film Dielectric Polymer-Based Inks

Dielectric inks are utilized to pattern insulating structures, where both pattern area and film thickness are variables of interest. Dielectric inks were first developed for inkjet printing with the purpose of creating thin dielectric films for metal-insulator-metal (MIM) capac-

itors and transistor gate dielectrics, yielding thicknesses in the ranging from hundreds of nanometers of several micrometers[22, 23]. However, the ability to print thick dielectric structures is integral to the realization of fully-printed antenna structures and wireless systems.

Commonly used as a photoresist in integrated circuit (IC) fabrication, SU-8 is a long-chain polymer that is deposited through spin-coating onto silicon wafers for electronic device patterning. Recent advances in inkjet printing have allowed for this polymer to go beyond its typical cleanroom use as a sacrificial mask towards a thick film dielectric for microwave devices [24, 25, 26]. SU-8 polymer chains have two advantages for inkjet printing fabrication: low-temperature UV cross-linking and high polymer content by weight while still maintaining a relatively low viscosity [27]. Low-temperature processing is useful when dealing with organic substrates typically used with inkjet printing that may deteriorate at higher temperatures, such as paper and LCP. High polymer content allows for a thicker, more uniform layer-by-layer deposition, while low viscosity is required to be compatible with industrial inkjet printer cartridges. In order to ensure viscous compatibility, SU-8 ink is formulated with the addition of a cyclopentanone solvent, as presented in Table 2.2 [28]. Once deposited, standard cleanroom baking and cross-linking procedures are performed to finalize the patterned dielectric film. Table 2.3 outlines a few DC electrical properties measured from inkjet-printed SU-8 films.

Table 2.2: Viscosity versus SU-8 polymer content within cyclopentanone solvent for SU-8 ink formulation.

Polymer w/w% in C_5H_8O	Viscosity (cP)
0	2
29	7.5
31	8
33	9
35	13

The microwave properties of the SU-8 polymer are advantageous for use as a thick dielectric film, with a relative permittivity of approximately 3.1 and a loss tangent of 0.04 up

Table 2.3: Summary of SU-8 dielectric film electrical properties

Relative Permittivity (ε_r)	Leakage Current Density (10 V)	Breakdown Voltage
3.75	$1.98\,\mathrm{pA/mm^2}$	$420\,\mathrm{V}$

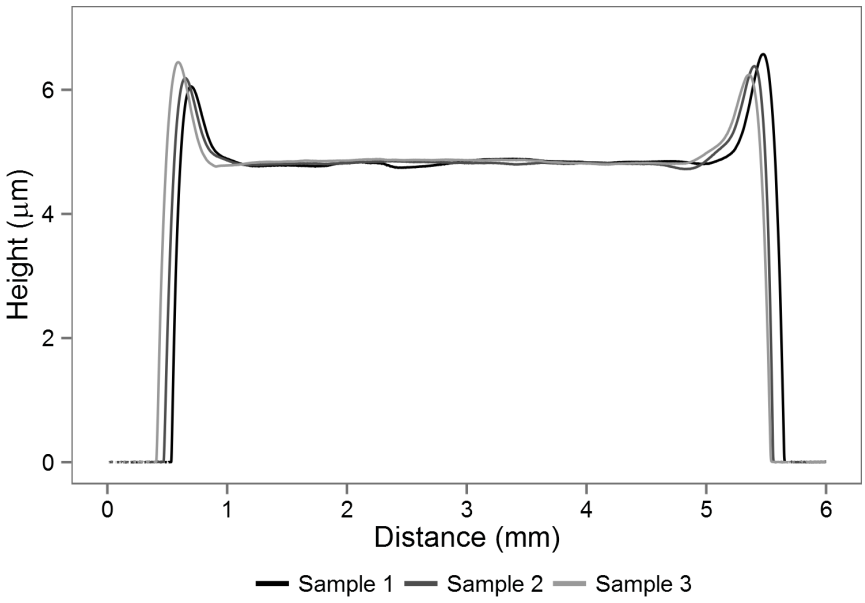


Figure 2.3: Profilometer measurements of printed single-layer SU-8 films.

to $40\,\mathrm{GHz}$ [29, 26]. SU-8 films can be deposited with a thickness of 4–$6\,\mu\mathrm{m}$ per layer using a $20\,\mu\mathrm{m}$ drop spacing, shown in Figure 2.3. The nonuniformity in the profile of printed SU-8 thick films is known as the "coffee ring effect" and is the result of surface tension mismatches between the deposited ink and the host substrate as well as material drying profiles [19]. Special surface treatment and variable baking temperatures are commonly used to minimize issues with SU-8 film uniformity and allow for the fabrication of uniform printed dielectrics exceeding $100\,\mu\mathrm{m}$ in thickness, which will be discussed further in Section 4.1.1.

2.2 3D Printing Techniques

3D printing is an additive manufacturing technology with a broad catalog of processes that vary in materials, resolution, and speed. Generally, 3D printing involves the layer-by-layer

formation of a 3D object using an additive tooling methodology. This is achieved through the process of "slicing" a 3D object model, where cross-sectional layers of specific Z height are discretized and subsequently printed. Three 3D printing methods are highlighted below with a focus on implications for electronic fabrication:

1. *Fused Deposition Modeling (FDM)* – Material filaments, typically thermoplastics, are extruded through a heated nozzle at a temperature that exceeds the filaments' glass transition temperature. Objects are formed through layer-by-layer deposition, where surface roughness and resolution are generally reliant on layer height and nozzle width [30].

2. *Stereolithography (SLA)* – An ultraviolet (UV) light source selectively patterns layers directly onto a flat build plate immersed within a vat of photopolymer resin. The UV source may consist of a rasterizing laser or digital light processing (DLP) based projection, where layers of the 3D object are subsequently cross-linked upon exposure. SLA 3D printing typically offers higher resolution and lower surface roughness due to optical processes, along with a greater part strength from the nature of layer-by-layer cross-linking.

3. *Selective Laser Sintering (SLS)* – A laser is used to selectively fuse a powder-based composite into a solid 3D object in a layer-by-layer fashion. SLS enables the direct 3D printing of metallic objects, however the powder sintering process presents challenges with surface roughness and high porosity.

2.2.1 SLA 3D Printing Process

The efforts presented in this thesis focus on the use of SLA 3D printing techniques for packaging solutions due to its attractive qualities of low surface roughness, high resolution, homogeneous object formation through resin cross-linking, and potential for high-throughput scalability, specifically within the class of DLP-based printing technologies.

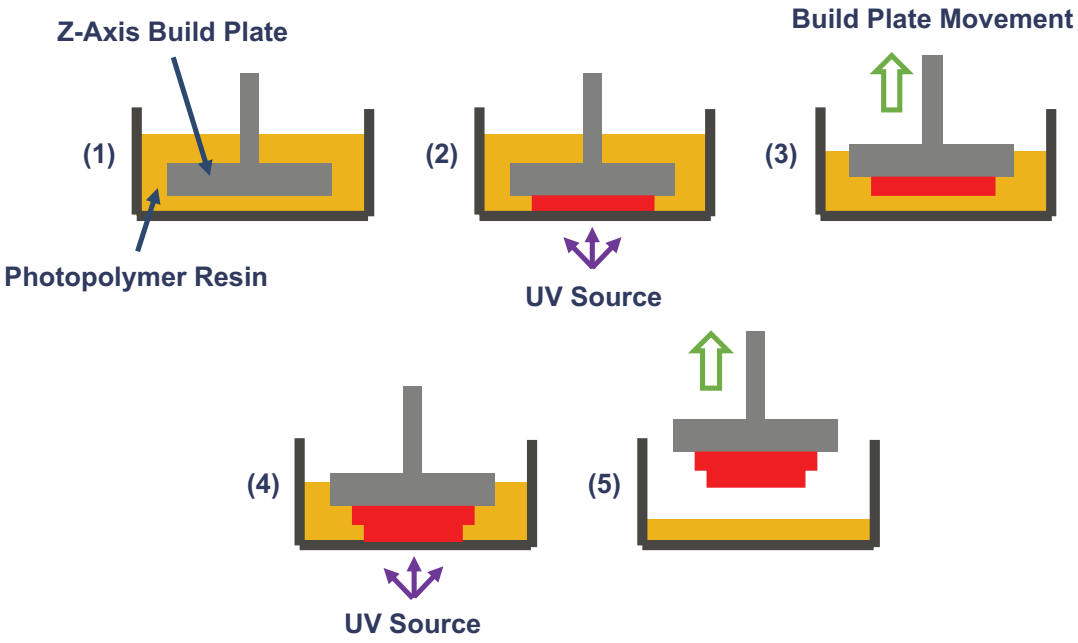


Figure 2.4: Stereolithography (SLA) 3D printing process diagram. (1) Starting position for first layer. (2) First layer exposure. (3) Build plate movement for next layer. (4) Subsequent layer exposure. (5) Final removal of 3D part from resin bath.

Fig. 2.4 presents a generalized process flow for SLA 3D printing. DLP-based SLA printing is targeted over a laser-based procedure in order to achieve a higher X/Y resolution with a lower cost of entry. A custom DLP-based LittleRP SLA 3D printer is selected as an effective platform utilizing a Viewsonic PJD7820HD, a 1080p DLP projector. The exposing projector is focused at a distance to provide $38\,\mu\mathrm{m}$ X/Y resolution based on the pixel size with $3000\,\mathrm{lm}$ intensity over a $41.5\times72\,\mathrm{mm}$ stainless steel build plate.

2.2.2 Photopolymer Resin Characteristics

The materials used with SLA printing consist of photopolymer resins that crosslink through exposure to ultraviolet (UV) and near-UV radiation (300–$400\,\mathrm{nm}$). Vorex (orange color) from MadeSolid and Porcelite from Tethon3D are photoresins designed to cure at UV wavelengths between 350–$410\,\mathrm{nm}$. Vorex is an acrylate-based resin focused on impact strength and toughness. Porcelite is a crystalline silica-loaded resin with the ability to fire at $1000\,^{\circ}\mathrm{C}$ into a fully porcelain object, however the inclusion of ceramic composites in the

resins have to potential to allow for an increase in permittivity to enable use as a dielectric for applications where firing is not desired.

Printed layer thickness is determined by the Z-axis stepper motor and is chosen to be $50\,\mu\mathrm{m}$ for a balance of resolution and processing speed. The $50\,\mu\mathrm{m}$ layers are exposed for $7\,\mathrm{s}$ to cure Vorex and $15\,\mathrm{s}$ to cure Porcelite. After all layers are exposed and printed, the samples are submerged in two isopropyl alcohol (IPA) baths in order to remove the majority of the residual unexposed material and then any remainder from the first bath. Finally, a post-print $1\,\mathrm{J/cm^2}$ UV exposure is performed to fully cure the 3D-printed Vorex and Porcelite parts.

CHAPTER 3
REVIEW OF MM-WAVE SIP ARCHITECTURES

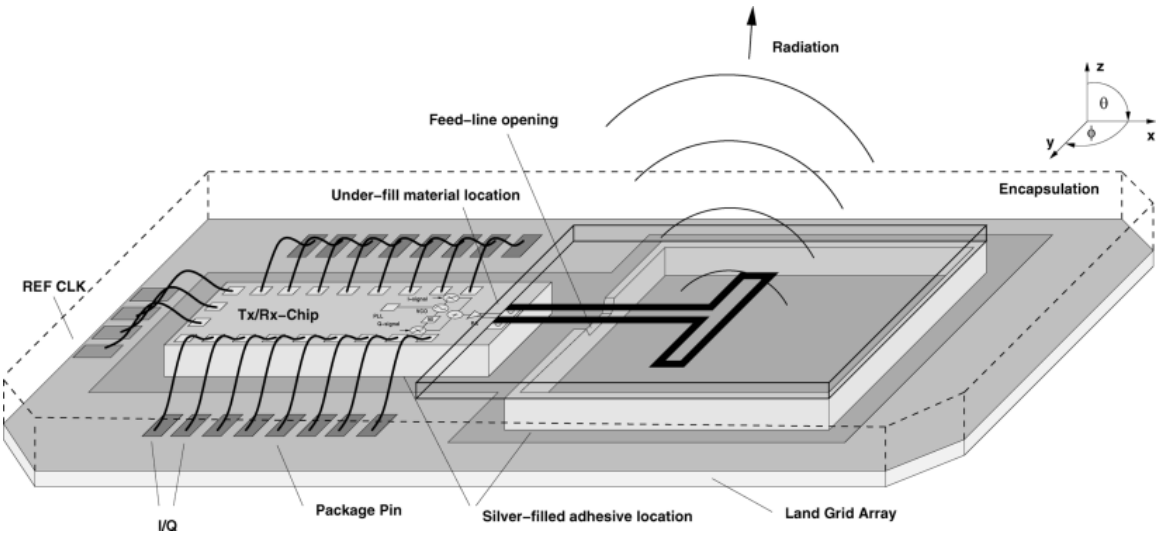
Two of the fundamental components of a wireless mm-Wave system package highlighted in this review are antennas and RF interconnects. Antennas are elements specifically designed for the conversion of circuit-based transmission line modes to wirelessly-radiated electromagnetic waves. Interconnects are signal paths responsible for the routing of RF signals between discrete circuit components within an RF package, including amplifiers, passive elements, and antennas. In order to address the challenges present in the design and utilization of mm-Wave hardware, novel integration schemes such as system-on-chip (SoC) and system-in-package (SiP) have garnered attention as enabling technologies, where essential system-level components, such as antennas, active devices, and passive peripherals, are all integrated into a single chip (SoC) or package (SiP). These methods reduce board-level assembly overhead and losses between components while simultaneously promoting system miniaturization, facilitating adoption into the small form factors of modern wireless devices. With the adoption of SiP technology with wireless systems, efforts are also pushing towards the integration of antennas within microelectronic packages to further reduce interconnection losses and improve the crucial link between a wireless device's first point-of-contact, the antenna, and the front end of an RF module. In this chapter, historical and current state-of-the-art efforts are reviewed for the development of Ka- (26.5–$40\,\mathrm{GHz}$) and E-band (60–$90\,\mathrm{GHz}$) package-integrated antennas and interconnects realized through both traditional and additive manufacturing-based fabrication methods.

3.1 mm-Wave SiP Antenna Design and Integration

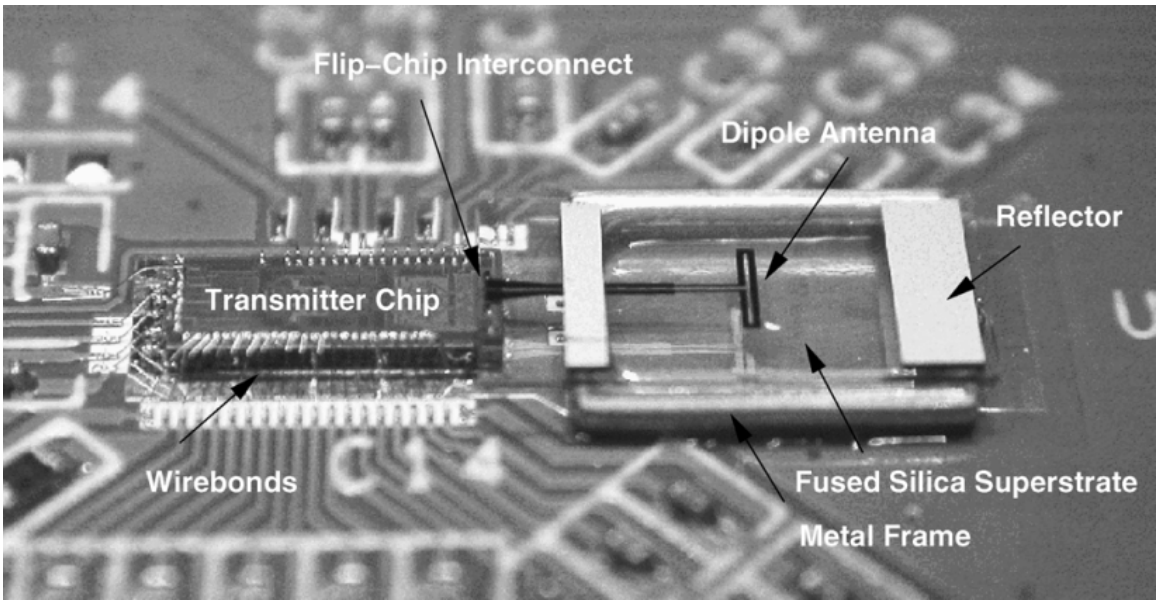
The integration of mm-Wave antennas within wireless microelectronic packages has been an emerging topic of research in the past few decades. In 1995, D. Griffin and A. Parfitt

outlined various electromagnetic considerations dealing with the integration of antennas within monolithic microwave IC (MMIC) packages, highlighting the necessity of shielding between active ICs and antenna elements as well as close attention to the orientation and spacing of phased array elements within a package [31]. Nearly a decade later in 2004, R. Carrillo-Ramirez and R. Jackson presented a packaging scheme involving the integration of a $39\,\mathrm{GHz}$ cavity-backed patch antenna array with a down-converting GaAs MMIC utilizing an etched silicon host substrate with a novel benzocyclobutene (BCB) spin coating and gold bump process [32].

Later that year, researchers with the IBM T.J. Watson Research Center in collaboration with the Georgia Institute of Technology presented a conceptual drawing of a fully-integrated SiGe-based mm-Wave transciever including a separate flip-chip mounted antenna within a quad flat no-leads (QFN) package, highlighting the potentially attractive features of package-level integration for reduced cost, power consupmotion, and losses from external interconnects [33]. In 2006, U. Pfeiffer with the IBM team presented a $60\,\mathrm{GHz}$ radio chipset with integrated folded dipole antenna and fused silica superstrate, demonstrating direct-chip-attach (DCA) and land-grid-array (LGA) solutions in a substrate-independent surface mount technology, realizing the novel antenna packaging co-design proposed two years prior [34]. A fabricated DCA assembly with a transmitter MMIC is shown in Fig. 3.1, featuring a flip-chip interconnection method for SiP integration [35]. This effort was followed by many achievements from the IBM team in collaboration with various institutions across the world, demonstrating package-integrated mm-Wave antennas featuring air cavities and aperature coupling in multilayer oraganic- and LTCC-based packages [36, 37, 38]. Today, single-package mm-Wave transceiver solutions are available in a variety of platforms for automotive radar and high-resolution remote sensing applications [39, 40, 41, 42, 43].



(a)



(b)

Figure 3.1: (a) Conceptual drawing of LGA MMIC package with integrated antenna, (b) fabricated DCA MMIC package with integrated antenna [35].

3.2 mm-Wave SiP Antenna Fabrication with Additive Manufacturing

With the mm-Wave wireless packaging scheme of SiP antenna integration entering mature commercialization, emerging research efforts tend to highlight two tracks: improving interconnection methods and broadening integration through expanding manufacturability. mm-Wave interconnection methods will be discussed in the following subsections, so this subsection will focus on the integration of additive manufacturing technologies, specifically inkjet and 3D printing, for the SiP integration of antennas within mm-Wave wireless systems.

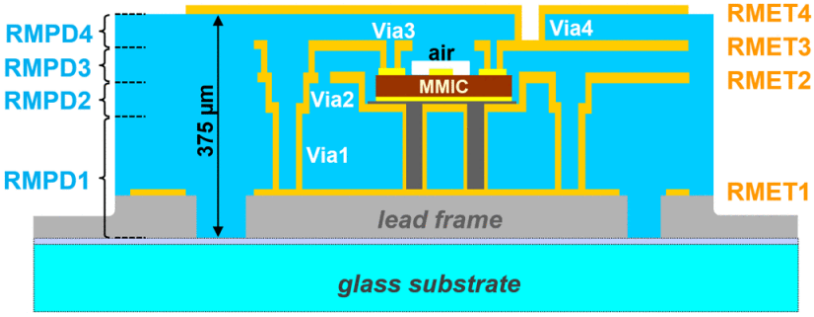
Additive printing techniques for antenna fabrication have evolved substantially in the past decade. First-generation efforts from the ATHENA Lab at the Georgia Institute of Technology demonstrated the feasibility of using inkjet printing to fabricate UHF (850–$960\,\mathrm{MHz}$) RFID tags on paper substrates, highlighting rapid low-cost production for massive-scale sensing and monitoring [12, 44]. In 2010, G. Shaker et al. presented a dual-band monopole antenna targeting $24/60/70\,\mathrm{GHz}$ wireless bands achieved through inkjet printing silver nanoparticle ink on a liquid crystalline polymer (LCP) host substrate, demonstrating that the limited feature resolution of low-cost printing technologies are adequate for the fabrication of mm-Wave antennas [45].

Up to now, a variety demonstrations of additively-manufactured mm-Wave antennas have been presented in literature, including $24.5\,\mathrm{GHz}$ proximity-coupled patch and Yagi-Uda arrays utilizing multi-material conductor/dielectric inkjet printing [29, 46]. Printed mm-Wave antennas have also been demonstrated with fully-printed mm-Wave balun structures to facilitate measurement and promote integration with typical microstrip-fed PCB technology [46, 47]. However, the integration of printed antennas with active MMIC devices is still a developing field with much progress to be made. An on-chip inkjet-printed monopole antenna integrated with a $24\,\mathrm{GHz}$ CMOS oscillator was presented by F. Ghaffar et al. in [48], however minimal performance characteristics were reported likely due

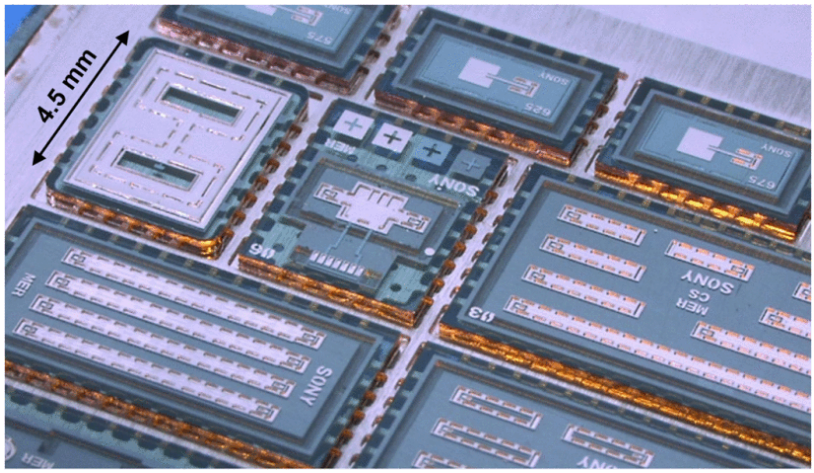
to the difficulty of achieving a high efficiency with an on-chip antenna. A novel 3D-printing approach utilizing mask-defined photo-polymerization was presented by T. Merkle et al, demonstrating the development of printed D-band (110–170 GHz) multi-chip modules (MCMs) with integrated SiP antennas and interconnects directly onto a metallic QFN leadframe, as seen in Fig 3.2 [4]. This "rapid micro-product development" (RMPD) masking approach achieves high resolution features in the range of several microns with the ability to realize dielectric structures with thickness ranging from one to hundreds of microns, however it is limited in cost-effectiveness and scale flexibility due to the necessity of masks for the patterning of both dielectric and conducting features, where metallic features are achieved through physical vapor deposition (PVD).

3.3 mm-Wave Interconnect Design and Integration

First-level interconnects are required in order to interface a mm-Wave MMIC die with a packaging substrate and other electronic components within the same package. The two most popular methods of realizing these interconnections for mm-Wave systems are wire bonding and flip-chip techniques. Wire bonding is a relatively cheap and flexible interconnection option involving the thermosonic bonding of a thin metallic wire, typically gold or more recently copper, with a diameter as small as one half of a mil (12.5 µm). The impedance of a ground-signal-ground (GSG) bond wire configuration is determined by the diameter and spacing of the wires, which in turn is a result of the GSG pad pitch of the interconnected MMIC device [49]. Though wire bonding is a wide-spread technology within microelectronic packaging, these interconnects are often prone to sway upon encapsulant molding and can suffer from high parasitic inductance, often requiring passive components for compensation at mm-Wave frequencies [37, 50]. Flip-chip techniques involve the deposition of solder bumps onto the pads of a die, where the die is then flipped onto a packaging substrate and then undergoes thermal reflow to provide interconnection. Though flip-chip techniques offer minimal interconnect lengths and consequent parasitics, practical imple-



(a)



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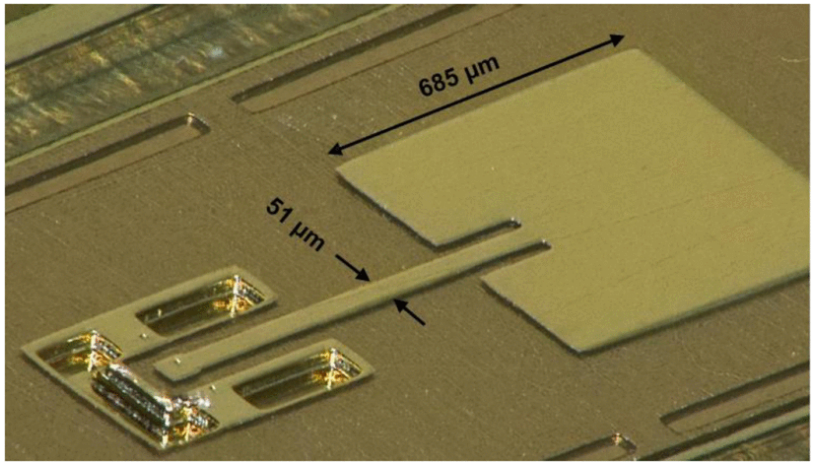


(c)

Figure 3.2: (a) Schematic cross section of a 3D-printed MCM device realized through the ”rapid micro-product development” (RMPD) masking manufacturing approach. (b) A batch of test structures fabriated on a QFN leadframe with the RMPD-mask approach, including D-band patch antennas, transmission lines, and waveguide launches. (c) D-band patch antenna detail. [4].

mentations are prone to suffer from high sensitivity to coefficient of thermal expansion (CTE) mismatch as well as detuning from the close proximity to on-package signal routing below the IC, due to the fact that the active side of the MMIC device is adjacent to the packaging substrate [2]. Because of the system-level design flexibility offered by wire bonding techniques for mm-Wave SiP schemes, wire bond interconnects will be the technology of comparison for the additive inkjet and 3D printing efforts of this thesis.

It should be noted that a direct comparison between the performance of mm-Wave interconnection techniques is a complicated task as there are many factors involved with determining the loss of a wire bond interconnect, including: (1) the package configuration (surface-mount or cavity-embedded) and (2) the wire bond height above the die/substrate and position of the pads, contributing to the total *loop length*. For example, G. Baumann et al. presented a cavity-embedded structure featuring an optimized $200\,\mu\mathrm{m}$ wire bond loop length yielding an insertion loss of $0.2\,\mathrm{dB}$ at $30\,\mathrm{GHz}$ [51]. Alternatively, Lim et al. present a surface mount DCA assembly featuring three $500\,\mu\mathrm{m}$-length wirebonds in a GSG configuration yielding an insertion loss of approximately $1.5\,\mathrm{dB}$ at $20\,\mathrm{GHz}$ [52]. For this reason, it is inadequate to judge the efficiency of an interconnection method based strictly on the *dB/mm loss* of an interconnect, which is a popular metric in literature. Ultimately, an ideal interconnect would be achieved with the shortest possible transition length and minimal impedance discontinuity between board and MMIC.

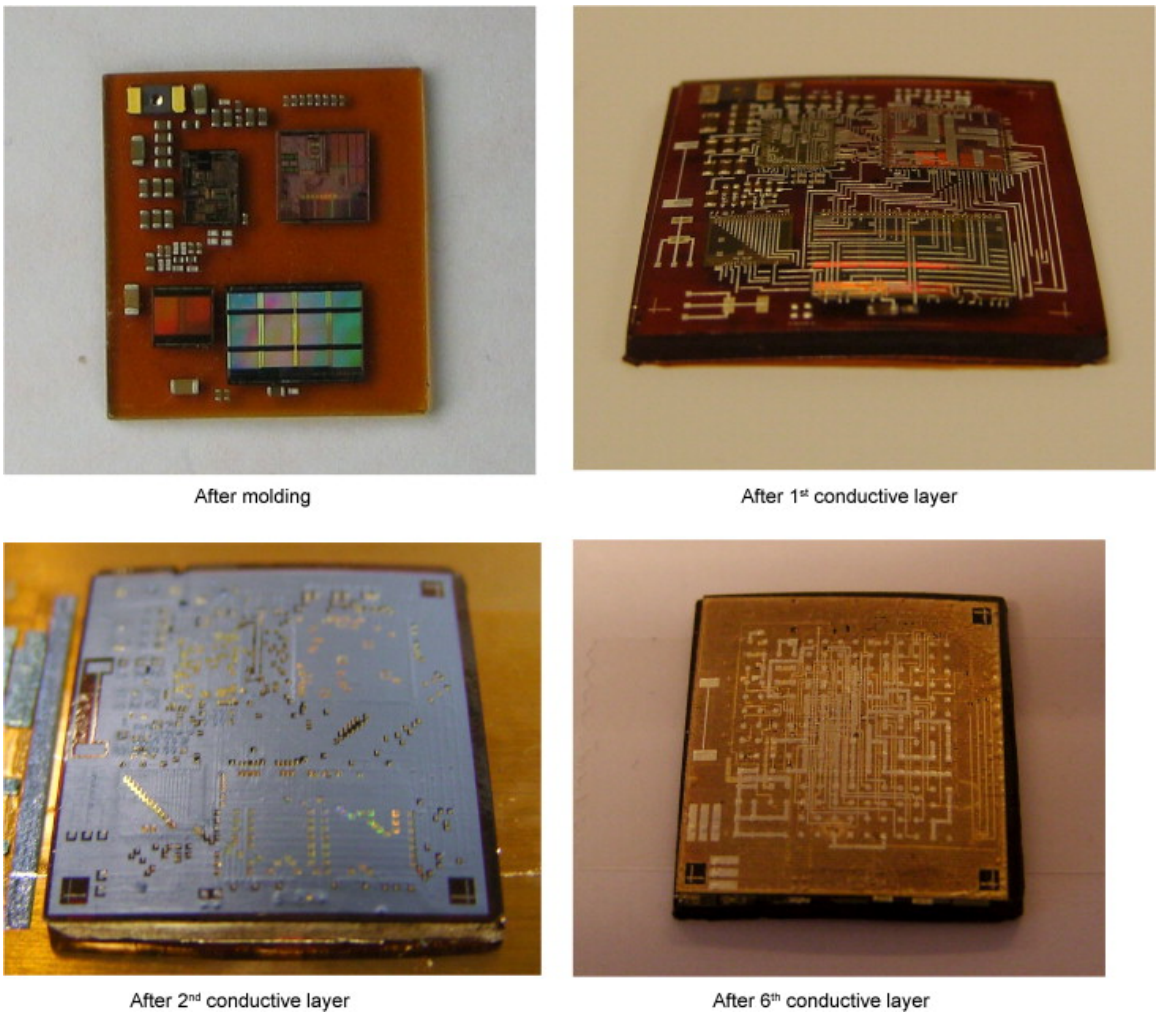
3.4 mm-Wave Interconnect Fabrication with Additive Manufacturing

As tooling technology within the field of additive manufacturing advances in both resolution and material diversity, direct interconnection with active MMIC devices has grown into a practical application with a variety of potential benefits for the challenges currently faced in the development of efficient mm-Wave device packages and systems. Specifically, the conformal layer-by-layer nature of inkjet printing offers a reduced 3D profile compared to traditional wire and ribbon bond interconnects, which can effectively lead to a decrease

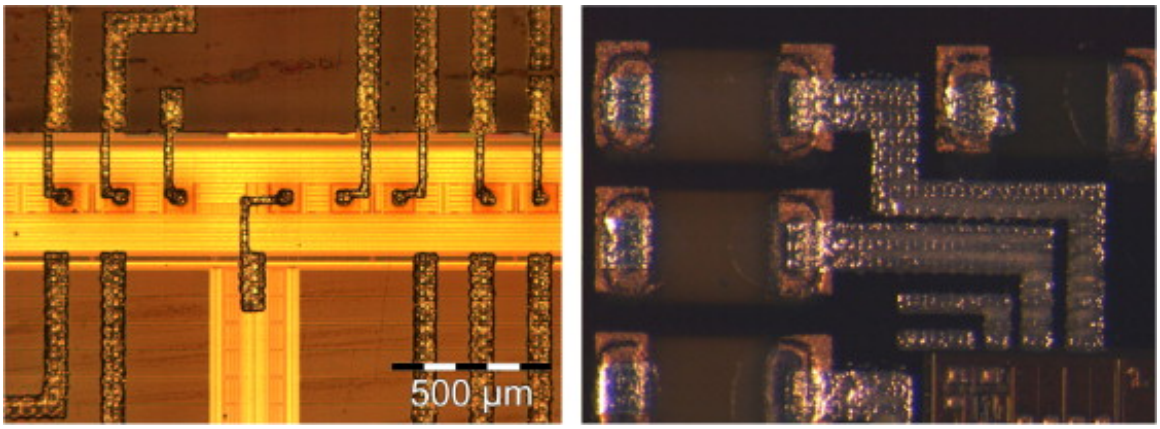
in impedance mismatch and inductance for the first-level transition and therefore improve matching and reduce parasitic losses.

Initial demonstrations of additively-manufactured first-level IC interconnects were explored by D. Hayes and other engineers with MicroFab Technologies. In 1999, D. Hayes et all reported the use of a high-temperature inkjet-based printing process, known as Micro-Jet, to selectively pattern solder bumps and vertical vias directly onto an IC in a chip-scale packaging (CSP) scenario [53, 54]. Several years later, H. Imai et al. from Seiko Epson demonstrated the use of embedded chips and inkjet-printed interconnects for a system-in-board (SiB) radio-controlled watch module [55]. Concurrently, H. Saito and T. Matsuba of Harima Chemicals' Tsukuba Research Laboratory presented an SiP LED driver module utilizing inkjet-printed silver NanoPaste interconnects with a bottom-up resin-molded package [56]. Soon after, collaborative efforts between Tampere University of Technology and the Nokia Research Center presented several demonstrations of SiP modules with inkjet-printed interconnects to surface-mount components and IC dies embedded within a resin mold [57, 58, 59]. These printed SiP modules, shown in Fig. 3.3, required all components to be placed active-side-up in a planar fashion, thus limiting 3D integration and recalling the challenges previously discussed with flip-chip interconnection methods.

In contrast to the approach of printing/molding a full module, research efforts began to shift towards demonstrating an efficient alternative to traditional interconnection methods for ICs. In 2010, M. Mengel and I. Nikitin explored the possibility of inkjet printing a polyimide dielectric ramp-like line structure to act as a 3D transition to the top of an IC die [60]. However, at this time interest began to grow with the maturity of aerosol jet printing systems from Optomec, where their researchers were able to demonstrate the use of aerosol jet technology to fabricate 3D interconnects for stacked-die packages utilizing a dispensed underfill adhesive as a dielectric ramp [61, 62]. Additionally, this method of interconnect fabrication was presented by T. Seifert et al. in 2015 for the development of MEMS stacked-die sensor module [63].



(a)



(b)

Figure 3.3: (a) Printed active-side-up SiP module at different stages of fabrication, (b) detail micrographs showing inkjet-printed interconnects to (left) IC pads and (right) 0402 capacitors [58].

Only in the past few years have research efforts begun targeting RF and specifically mm-Wave interconnection applications. The first demonstration was presented by the author in 2016 where inkjet printing was used to pattern 3D dielectric ramps and metallic interconnects to a blank silicon die, as well as interconnect to a Ka-band in-package antenna in an SiP fashion [7]. Soon after, a combination of inkjet and stereolithography (SLA) 3D printing was used to demonstrate 3D arbitrarily-sloped interconnects, including characterization up to $67\,\mathrm{GHz}$ [64]. Efforts with aerosol jet printing for mm-Wave interconnection and packaging have been growing as well, including recent work from M. Craton et al. demonstrating a chip-first approach with fully-printed substrate and interconnects for a GaAs attenuator MMIC [65]. Today, the integration of printed interconnects with active MMIC devices, such as low noise amplifiers (LNA), power amplifiers (PA), and switches is just beginning to be evaluated [66].

CHAPTER 4

MM-WAVE ANTENNA INTEGRATION

As the demand for mm-Wave wireless hardware grows for emerging communication and remote sensing applications, engineering efforts are highlighting the need for advanced and efficient integration techniques at the system level. The SiP design approach has been demonstrated as a promising candidate for these systems, where the reduction and potential elimination of various discrete connectorized modules enables system miniaturization while mitigating losses between individual MMIC devices and necessary peripheral components. Furthermore, the level of integration between the antenna and the RF front-end module is of specific interest, where this highly sensitive path is essential for the efficient receiving and transmitting of wireless signals. The ability to reduce the losses of these transitions and ensure proper matching throughout remain a goal of the SiP approach, where on-package antenna architectures and heterogeneous integration provide a solution for the wireless system at the back-end-of-line and package level.

The on-demand nature of additive manufacturing allows for the selective deposition of RF materials and circuits on a virtually limitless variety of host materials. Though there have been demonstrations of inkjet printing technology on such substrates as glass, LCP, and paper, there still exists the need to distance electronic fabrication from a select catalog of RF substrate materials. In such applications such as on-chip wireless communication and SiP wireless architectures, system integration and 2.5D/3D design schemes are limited to existing subtractive fabrication techniques, which rely on the constraints of the surrounding laminate-based topology. It is desired to have the ability to fabricate and assemble wireless modules that are independent and versatile in both material stack-up and electrical aspects. The acquisition of this capability facilitates the achievement of ultra-miniaturized wireless systems which require extremely high integration of RF and other device components.

This chapter focuses on the design and implementation of inkjet printed mm-Wave antennas and arrays for SiP design schemes. First, the development and characterization of inkjet-printed thick dielectric films is outlined and used for the first realization fully-printed RF substrates and stack-ups. These advanced manufacturing methods are then applied to the design and fabrication of high gain mm-Wave proximity-coupled patch and Yagi Uda arrays, utilizing printed dielectric films as selectively-patterned RF substrates to achieve the highest gain inkjet-printed antennas in the mm-Wave regime at the time of publication. Finally, the patterning of a fully-printed mm-Wave patch antenna is demonstrated directly onto a molded IC package, presenting a new level of integration for fully-printed antennas and arrays in a SiP fashion.

4.1 Fully-Printed RF Substrates and Vias

In order to establish a robust printing scheme for multilayer antenna structures, several processing techniques must be employed for use with thick film polymer-based inks [28]. A dielectric structure used for this purpose must be able to be deposited in an efficient, uniform manor in order to ensure both predictability with modeling and reliability with fabrication. These goals can be achieved through the utilization of several advanced processing techniques discussed within this chapter. As a demonstration, fully-printed RF structures are also presented, where all multilayer components (ground, dielectric substrate, vias, and microstrip topology) are realized through additive inkjet printing manufacturing.

Additionally, fully-printed vias, RF microstrip lines, and T-resonator structures are fabricated to characterize the SU-8 dielectric ink [26]. These structures are used demonstrate multilayer printed interconnects and extract the loss and relative permittivity of the printed SU-8 material from 0–$30\,\mathrm{GHz}$. The realization of thick dielectric substrates and vias with inkjet printing helps advance the development of fully-printed multilayer and substrate-independent antenna structures, further distancing design and fabrication from bulk laminate substrate restrictions.

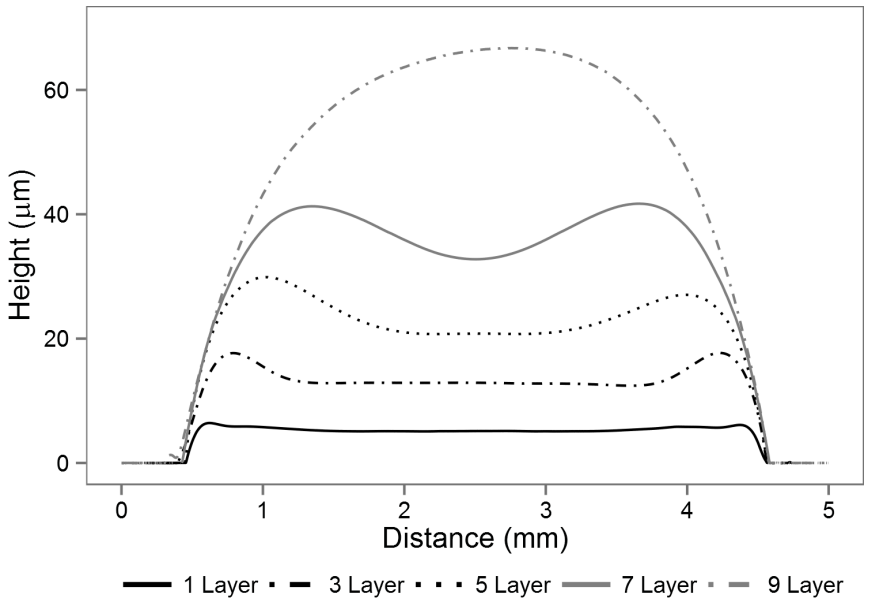


Figure 4.1: Profilometer measurements of printed multilayer SU-8 films.

4.1.1 Multilayer Printing Processes

As previously discussed, there are several issues present in the surface profiles of printed dielectric films that result from surface energy mismatches and material drying profiles. These issues have the potential to multiply with the printing of multiple layers, yielding thick dielectric substrates without uniform profiles, essentially reducing practicality for antenna structure fabrication. Profilometer scans of printed multilayer SU-8 dielectric films are shown in Figure 4.1 for 1-, 3-, 5-, 7-, and 9-layer prints using with $10\,\mathrm{pL}$ cartridges and $20\,\mu\mathrm{m}$ drop spacing. As the number of printed layers increases, the "coffee ring" profile tendencies present in single-layer prints merge into larger-scale profile uniformity issues, where variation in the range of 20% of total printed thickness can be witnessed, for example with the 7-layer print in Figure 4.1. In order to assess this issue and improve profile uniformity throughout a printed film while ensuring multilayer printing capabilities, several advanced processing techniques can be employed: UV ozone surface modification, thermal reflow, and multi-session printing.

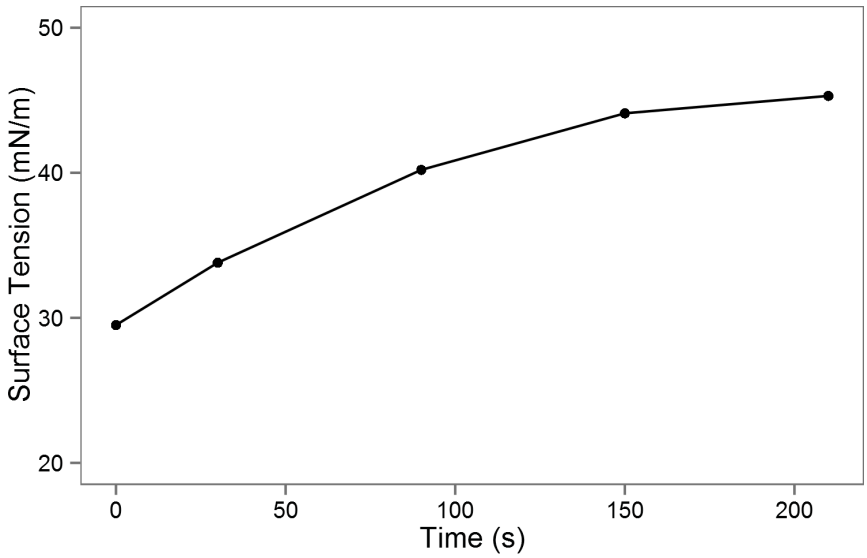


Figure 4.2: Surface energy measurements for printed SU-8 dielectric films with various durations of UV ozone exposure.

UV Ozone Surface Modification

The wetting of an ink droplet, no matter its chemical composition, is subject to the surface tension of the ink material and surface energy of the host substrate. As previously discussed, mismatches in these properties can result in ink droplets spreading or "balling-up" upon interaction with a substrate, often defining the integrity of a printed pattern. In order to tune this crucial interaction, the surface energy of a substrate can be modified and tuned with the use of UV ozone exposure. This process is especially important in the desired utilization of inkjet-printed dielectric films as multilayer RF antenna substrates.

In order to understand the interaction of ink materials with printed dielectric films, contact angle and surface energy measurements are performed on a printed SU-8 dielectric film. Figure 4.2 shows a parametric exposure of a printed SU-8 film with UV ozone exposures up to $210\,\mathrm{s}$ using a UVO Cleaner Model No. 42 provided by Jelight (Jelight Company Inc., Irvine, CA, USA). As exposure time increases, the surface energy of the printed SU-8 film approaches a saturation energy around $45\,\mathrm{mN/m}$. This process demonstrates the tunability of the surface energy of a printed-film in order to ensure proper wetting with

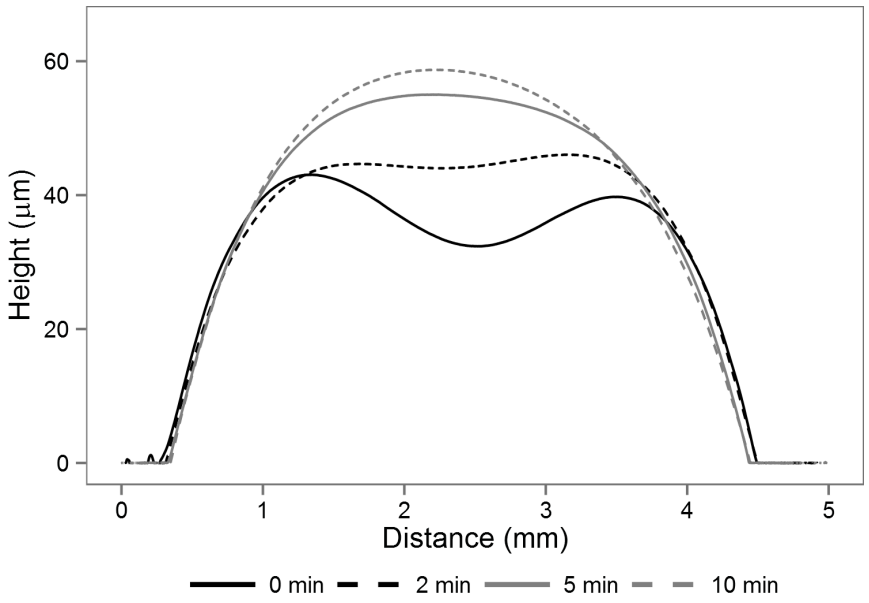


Figure 4.3: Profilometer measurements of printed SU-8 dielectric films with various durations of $150\,^{\circ}\mathrm{C}$ thermal reflow processing.

other inkjet printing materials, such as metallic inks, in order to realize multilayer printed structures.

Thermal Reflow

The surface uniformity of printed dielectric films is very important in the realization of multilayer printed structures. When multiple stacked topologies are desired, theses variations in uniformity have the potential to add and multiply of the process of the fabrication and cause great issue for overall system reliability. For this reason, it is desired to improve the profile uniformity of inkjet-printed films. This can be achieved through the use of a thermal reflow treatment on a printed polymeric film. The process begins directly after printing during the initial soft bake, where temperature is raised beyond the typical processing temperature to $150\,^{\circ}\mathrm{C}$. By increasing the temperature, the viscosity of the pre-cured film decreases, causing the profile to deform and the heightened edges of the film to settle into a more uniform shape. Figure 4.3 shows the result of a thermal reflow process on a printed SU-8 dielectric film for different durations of time. Both the initial shape of the film

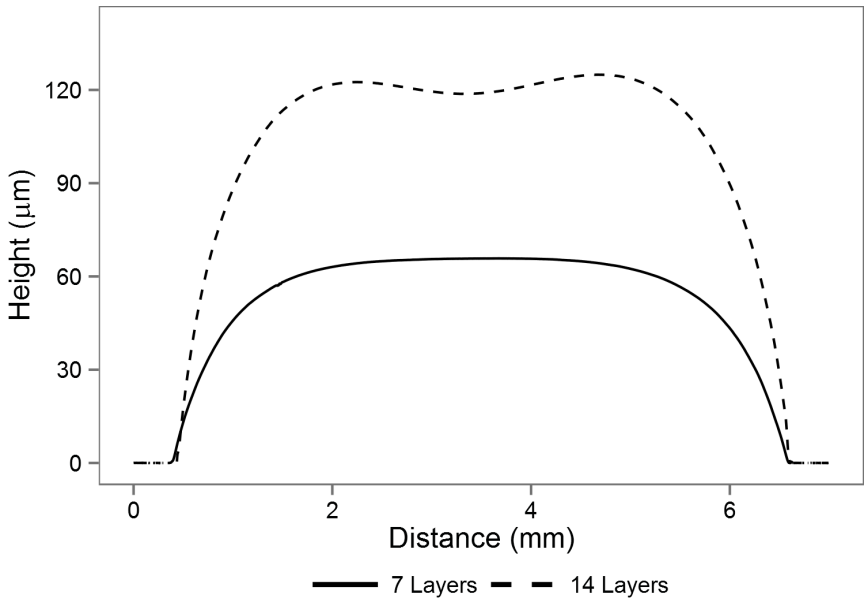


Figure 4.4: Profilometer measurements of printed SU-8 dielectric films with 7-layer and 7-layer + 7-layer (14 layers total) multi-sessions printing.

and the time of reflow are important parameters that must be considered when performing reflow processing. As is shown with the 5 and $10\,\mathrm{min}$ processing durations in Figure 4.3, excessive thermal processing can lead to over-deformation and a convex, nonuniform resulting profile. Once the desired profile is achieved during the thermal processing of the soft bake, standard curing processes are applied to finalize the patterning of the uniform dielectric film.

Muli-Session Printing

As previously discussed, the profile of an inkjet-printed dielectric film depends on several factors, including the area of the structure and the number or printed layers. When many layers of material are printed within a single area, profile deformities can arise, such as the 9-layer print shown in Figure 4.1. The large amount of material deposited within a certain area causes the film to bulge and create a convex drop-like structure. In order to avoid this nonuniform structure, multi-session printing can be utilized.

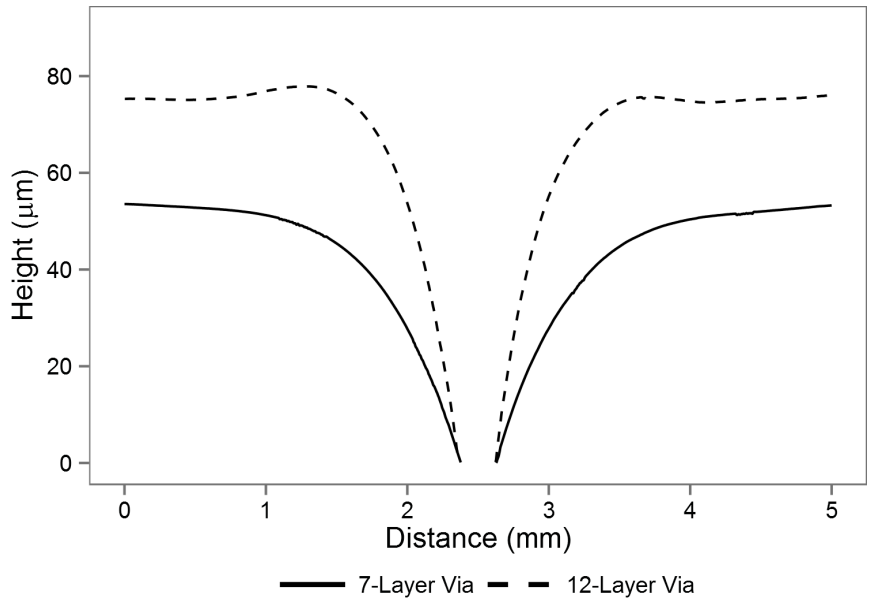
Multi-session printing involves the use of multiple printing and curing sessions to re-

alize thick, uniform dielectric structures without issues of material bulging. The process begins with an analysis of printed layer count and resulting film profile. Once a desired profile is achieved, typically involving the maximum amount of printed layers before a convex profile is formed, the printing session is repeated in order to yield the desired dielectric film thickness. Figure 4.4 shows profilometer scans of printed SU-8 dielectric profiles with multisession 7-layer prints [6]. Through the use of multi-session printing, uniform dielectric structures exceeding 100 μm are able to be realized with inkjet printing technologies for the selective patterning of thick dielectric substrates.

4.1.2 Multilayer Vias

From an additive approach, vias are constructed through a lack of material deposition in a small area. One issue with this additive approach of via fabrication is the presence of slanted walls on the edges of printed dielectric structures. Multi-session printing of dielectric layers increases the slope of the walls of dielectric structures, shown in Figure 4.5(a), helping to conform the shape of inkjet-printed vias to traditional vertical-wall vias. The ramp-up distance of the SU-8 sidewalls from zero thickness to the nominal dielectric thickness is found to be approximately 1 mm.

A test structure is fabricated in order to determine the DC resistance of the inkjet-printed vias. A 4-layer ($25\,\mu\mathrm{m}$) SU-8 dielectric structure with via holes is printed on top of ten traces of 4-layer ($3\,\mu\mathrm{m}$) Silverjet DGP-40LT-15C silver nanoparticle ink. Finally, 4-layer silver traces are printed on top of the dielectric substrate with and without the via connection to the bottom traces in order to determine the DC resistance of the ramp-up vias. A micrograph of an inkjet-printed via is shown in Figure 4.5(b). Comparing the DC resistances of the complete and incomplete traces, the printed samples yield an average DC resistance of $0.073\,\Omega$ with a standard deviation of $0.041\,\Omega$ for the $1\,\mathrm{mm}$ length ramp-up vias, which is an improvement on the efficiency [67, 68] and variance [69] of inkjet-printed vias presented in previous works. Table 4.1 provides a summary of the printed via DC



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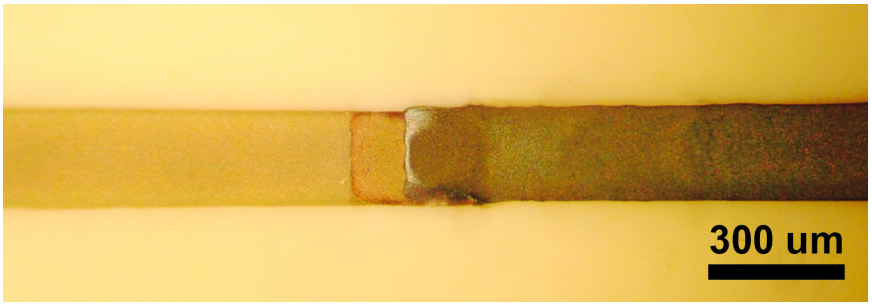


(b)

Figure 4.5: (a) Profilometer scans of inkjet-printed vias realized in 7- and 12-layer SU-8 dielectric substrates. (b) Micrograph of printed via transition test structure fabricated to measure DC resistance of ramp-up vias.

resistance measurements.

Table 4.1: Summary of Measured DC Resistances of Inkjet-Printed Vias

	Incomplete Lines (Ω)		**Completed Lines** (Ω)
	Top	Bottom	
	0.345	0.251	0.692
	0.328	0.267	0.617
	0.345	0.238	0.623
	0.310	0.241	0.693
	0.298	0.250	0.631
	0.361	0.251	0.685
	0.354	0.235	0.654
	0.364	0.252	0.606
	0.342	0.247	0.676
	0.286	0.238	0.660
Average	0.333	0.247	0.654
Std. Dev.	0.026	0.009	0.031
Via Average	0.073		
Via Std. Dev.	0.041		

4.1.3 Microstrip Line

To demonstrate the concept of using SU-8 dielectric ink as a thick RF substrate, a microstrip line is fabricated on a printed SU-8 film with Silverjet DGP-40LT-15C silver nanoparticle ink [26]. In order to allow for ground-signal-ground (GSG) probe feeding and measurements, a CPW-to-microstrip line transition is included in the design. The thickness of the SU-8 substrate is chosen to be $80\,\mu\mathrm{m}$ to yield a feasible microstrip line width and CPW gap ($100\,\mu\mathrm{m}$ spacing between signal and ground). The CPW-to-microstrip line transition is printed near the edge of the SU-8 substrate, where the CPW ground lines are extended down to the ground plane of the circuit. Images of the microstrip line with CPW-to-microstrip line transitions are shown in Figure 4.6.

In order to characterize the line loss and group delay of the microstrip line, a 37369A vector network analyzer (VNA) provided by Anritsu is utilized (Anritsu Company, Kanagawa, Japan). The effects of the probes and feed lines are de-embedded with the use of a printed TRL calibration kit following the same processing conditions. The line loss and group delay of the $6\,\mathrm{mm}$ microstrip line with respect to frequency are shown in Figure 4.7(a) and 4.7(b), respectively, from 1–$30\,\mathrm{GHz}$. The line loss increases as frequency increases because of an increase in dielectric loss and surface resistance. Additionally, radiation from the line also increases with frequency. The group velocity decreases slightly at lower frequencies yet remains fairly constant above $5\,\mathrm{GHz}$ up to $30\,\mathrm{GHz}$.

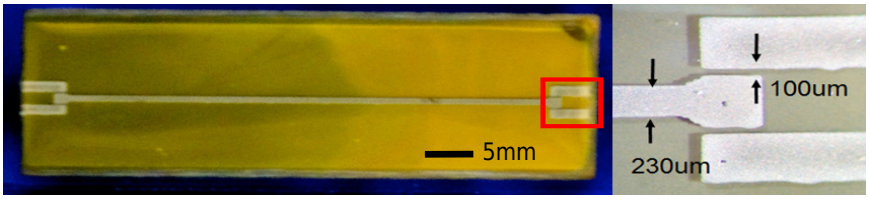
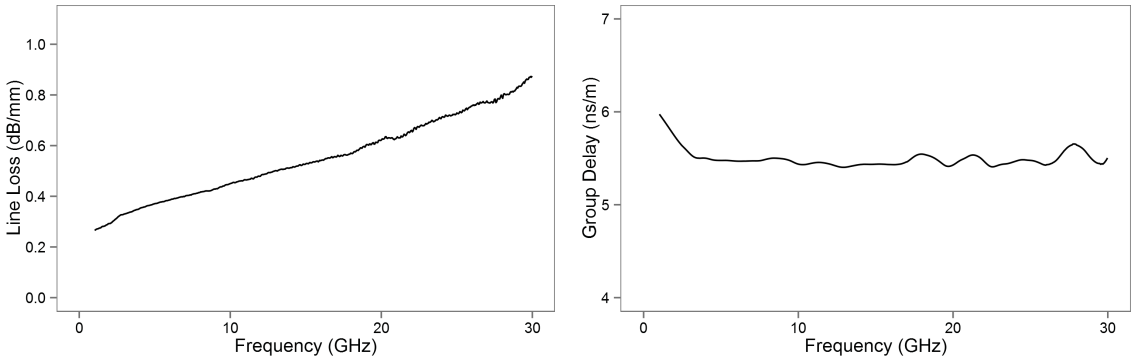


Figure 4.6: Micrographs of fully-printed microstrip line with CPW to microstrip line transition.



(a) (b)

Figure 4.7: Measurements of fuly-printed microstrip (a) line loss and (b) group delay as a function of frequency.

4.1.4 T-Resonator Characterization

Another structure commonly utilized for RF material characterization is the T-resonator, which can be easily fabricated using the multilayer process previously outline. As a proof-of-concept demonstration, a purely additive microstrip T-resonator with a fundamental resonant frequency at $2.21\,\mathrm{GHz}$ is utilized for the RF characterization of this completely inkjet-printed structure, consisting of a full ground plane, SU-8 dielectric substrate, and microstrip topology [26]. Figure 4.8 shows the fabricated T-resonator, including a microstrip transmission line with length $19.8\,\mathrm{mm}$ and a microstrip resonating line with length $19.5\,\mathrm{mm}$.

Using the harmonics of the resonant frequency at $2.21\,\mathrm{GHz}$, the T-resonator is used to extract the relative permittivity of the SU-8 substrate up to $30\,\mathrm{GHz}$. To validate the accuracy of the characterization, both T-Resonator and two line methods are adopted [70, 71, 72]. The relative permittivity values obtained through the use of these two methods are shown in Figure 4.9. Both of the results compare well with results gathered in previous works [73]. As frequency increases, measurements also agree with the expected trend in the material characteristics of the SU-8 dielectric, where the relative permittivity gradually decreases.

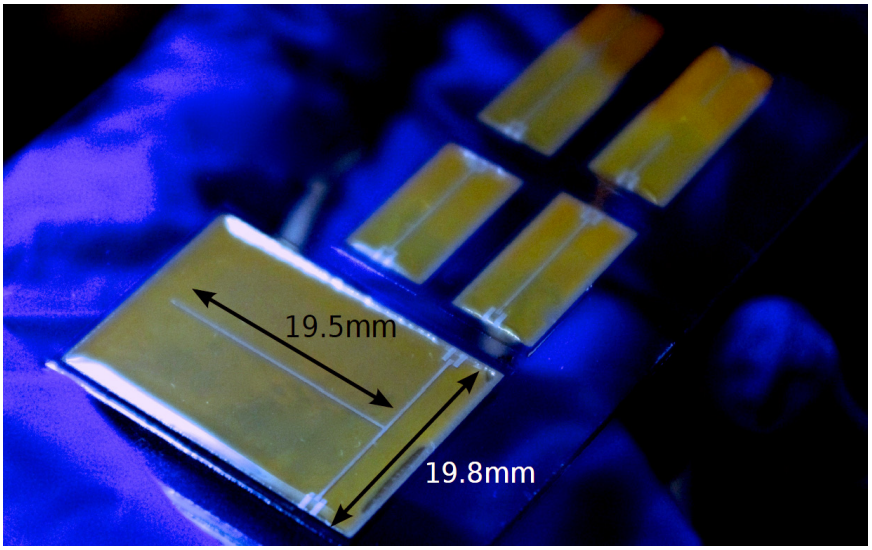


Figure 4.8: Image of fully-printed T-resonator, microstrip lines, and TRL calibration kit.

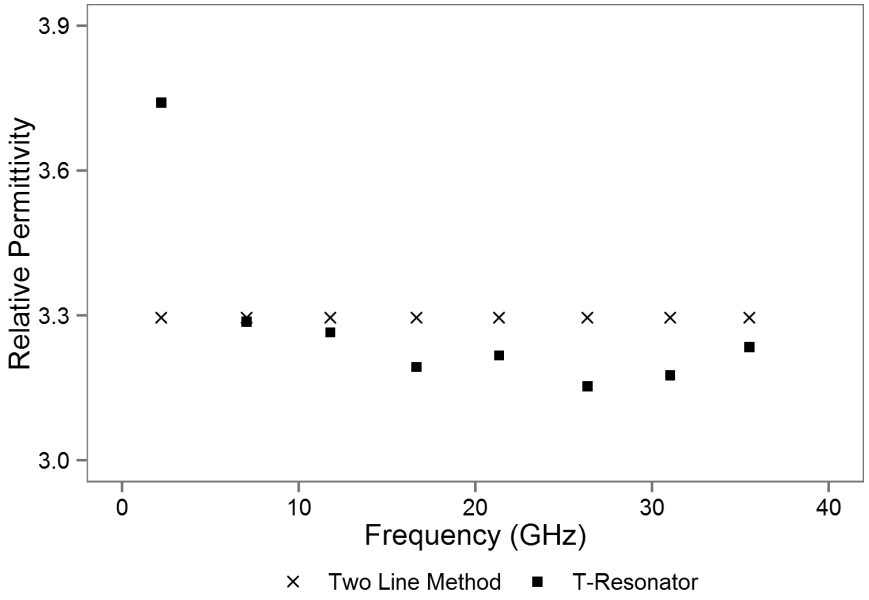


Figure 4.9: Measurements of relative permittivity for inkjet-printed SU-8 substrate.

4.2 Multilayer mm-Wave Antenna Arrays

The additive nature of this fabrication method allows for the development of multilayer, vertically-integrated antenna structures for use with flexible organic substrates, on-chip post-processing, and the use of novel low-temperature substrates while reducing fabrication time and material waste from traditional methods.

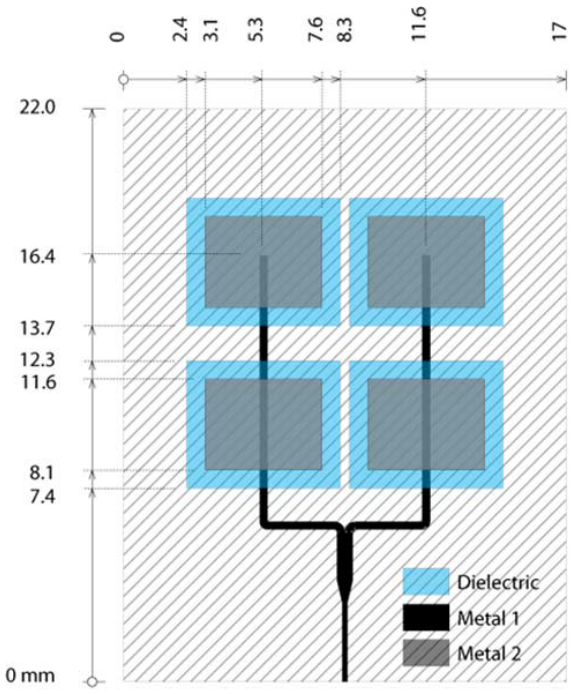


Figure 4.10: Topological model of $24.5\,\mathrm{GHz}$ proximity-coupled patch antenna array.

In this section, two multilayer inkjet-printed antenna structures are presented for operation within the $24.5\,\mathrm{GHz}$ ISM band. The first design is an adaptation of the canonical patch antenna array utilizing proximity-coupled feeding [29]. The second design is a Yagi-Uda antenna array featuring an unbalanced (microstrip) to balanced (slotline) excitation [46].

4.2.1 Proximity-Coupled Patch Antenna Array

To demonstrate the multilayer inkjet printing process with conductive and thick dielectric inks, a 4-element proximity-coupled patch antenna array is designed for use within the $24.5\,\mathrm{GHz}$ ISM band [29]. The proximity-coupled feeding technique improves the matching of the patch to the $50\,\Omega$ microstrip feed line while also increasing the bandwidth of operation. The patch arrays are modeled, simulated, and optimized within the CST Microwave Studio Suite, yielding an optimal center-to-center element spacing of 0.51λ in the horizontal direction and 0.6λ in the vertical direction. The dimensions of the patch elements are determined to be $3.5\times4.4\,\mathrm{mm}^2$. A model of the patch array is shown in Figure 4.10.

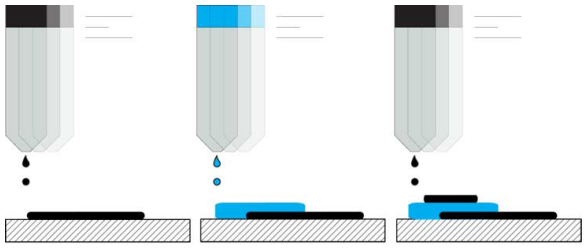


Figure 4.11: Fabrication process flow for inkjet-printed proximity-coupled patch antenna array showing the printing of silver (black) and SU-8 (blue) inks.

With traditional fabrication techniques, the proximity-couple patch array requires two laminate substrates: a host substrate and a dielectric spacer; along with three metallic patterns: a ground plane, microstrip feed lines, and resonant patches. Utilizing inkjet printing, the substrate is reduced to one material with selectively patterned dielectric spacers, avoiding any laminate bonding or subtractive patterning.

A diagram outlining the processes flow is displayed in Figure 4.11. Using a Dimatix DMP-2831 inkjet printing system, three layers of Cabot CCI-300 silver nanoparticle ink are printed onto a single-clad Rogers LCP substrate. The printed silver is then cured and sintered with the thermal baking profile outlined in Section 2.1.3 to finalize the microstrip feed lines. After sintering, the substrate is treated with $30\,\mathrm{s}$ of UV ozone exposure and 10 layers of SU-8 dielectric are printed to achieve the $60\,\mu\mathrm{m}$ spacer thickness. The SU-8 then undergoes a pre-exposure curing at $90\,^{\circ}\mathrm{C}$ for $5\,\mathrm{min}$, exposure to $365\,\mathrm{nm}$ UV light for cross-linking, and post-exposure curing at $120\,^{\circ}\mathrm{C}$ for $5\,\mathrm{min}$. After another UV ozone treatment for $90\,\mathrm{s}$, three silver layers are printed to pattern the top patches with curing and sintering profiles similar to the previous metal layer, concluding the fabrication process.

A micrograph image of the printed proximity-coupled patch array is shown in Figure 4.12. Physical measurements of the printed samples show good agreement with the model topology, with the exception of a dielectric thickness of $64\,\mu\mathrm{m}$, $4\,\mu\mathrm{m}$ greater than the desired dielectric thickness. The dimensions of the fabricated patch elements are measured to be $3.52\times4.5\,\mathrm{mm}^2$, yielding a maximum 2.3% variation from the initial dimensions.

Upon completion of fabrication, end-launch $2.92\,\mathrm{mm}$ connectors from Southwest Mi-

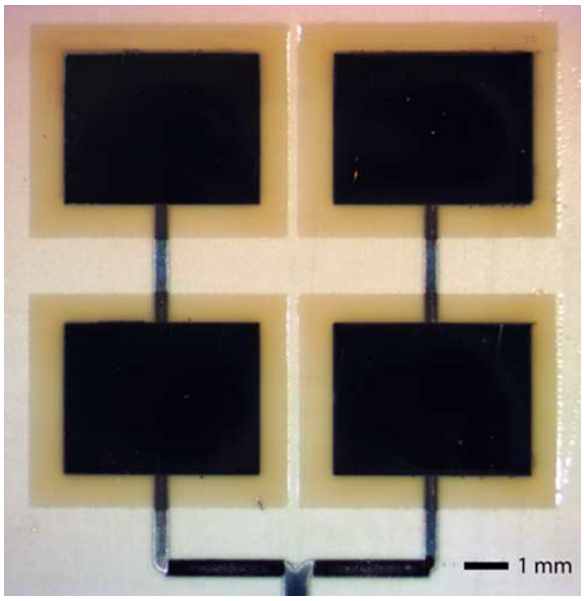


Figure 4.12: Micrograph of fabricated proximity-coupled patch antenna array.

crowave (Southwest Microwave, Tempe, AZ, USA) are mounted to the printed antenna and return loss of the samples is measured using an Anritsu 37369A VNA. Simulated and measured return loss is shown in Figure 4.13, showing good agreement with both printed samples at $24.75\,\mathrm{GHz}$. The frequency at which the fabricated antennas experience the best matching is approximately 1% higher than the intended frequency due to small fabrication variations, but good matching is achieved through post-fabrication simulation.

The radiation patterns and broadside realized gain of the printed arrays are measured within a far-field anechoic chamber utilizing standardized gain horns. The gain and pattern measurements are shown in Figure 4.14 and Figure 4.15, respectively. The measured magnitude of broadside realized gain matches well with the simulation, reaching up to $7\,\mathrm{dBi}$. Normalized E and H-plane radiation patterns show good agreement with simulations, with exception to the $180°$ direction due to the presence of the end-launch connector and its exclusion from simulations.

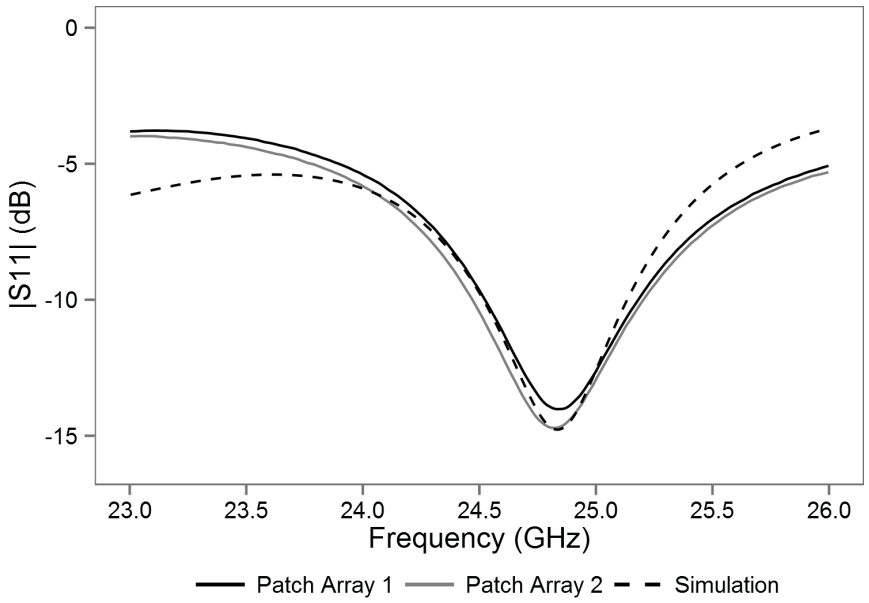


Figure 4.13: Simulated and measured return loss for printed patch arrays.

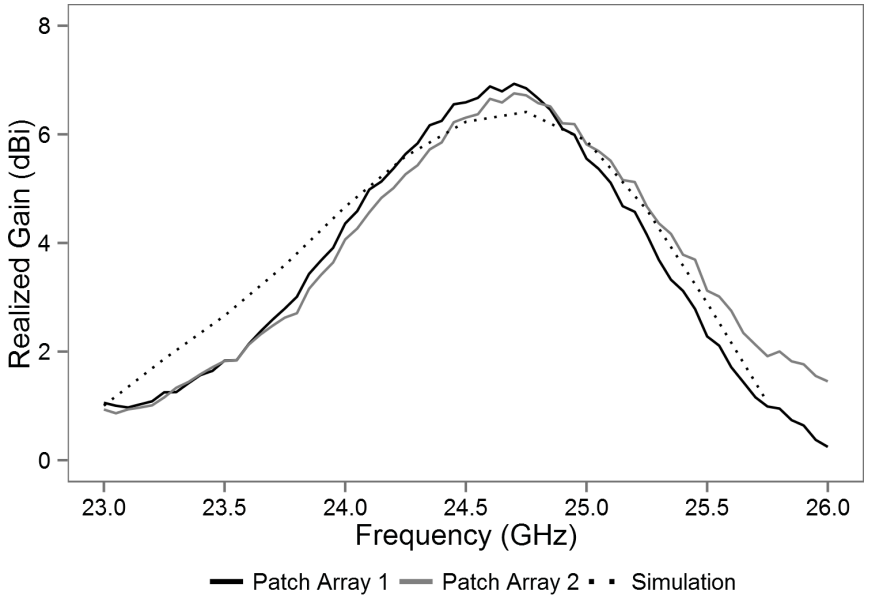
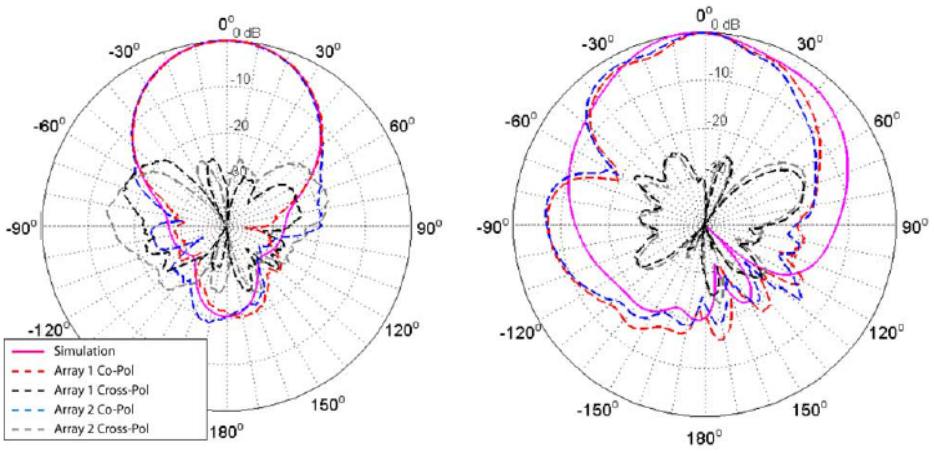


Figure 4.14: Simulated and measured broadside realized gain versus frequency of the proximity-coupled patch arrays.

4.2.2 Multilayer Yagi-Uda Antenna Array

As another demonstration of multilayer inkjet printing fabrication technology, multi-director Yagi-Uda antenna arrays are designed for the $24.5\,\mathrm{GHz}$ ISM band [46]. In order to reach a balance between end-fire gain and antenna size, 3- and 5-director topologies are modeled,



(a) (b)

Figure 4.15: Simulated and measured normalized (a) H-plane and (b) E-plane radiation patterns.

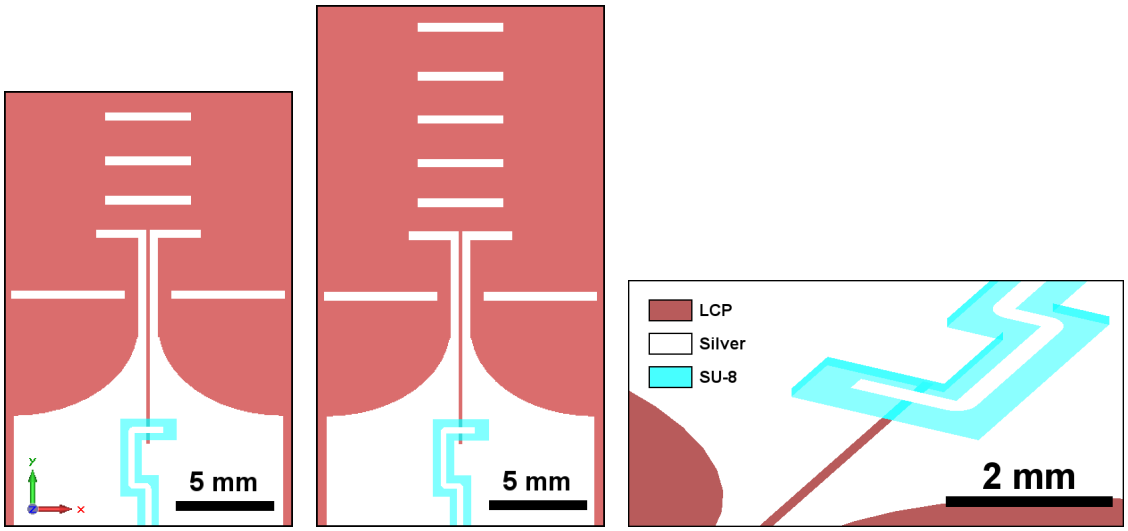
simulated, and optimized within the CST Microwave Studio Suite. The design includes a transition from a microstrip feed to a slotline feed for matching and test equipment integration [74]. A model of the 3- and 5-director Yagi-Uda arrays is shown in Figure 4.16.

The process flow for the fabrication of the Yagi-Uda arrays is the same as previously outlined for the proximity-coupled patch antennas in Section 4.2.1 with two deviations:

1. Unclad Rogers LCP is used.

2. 18 layers of SU-8 are printed to achieve a dielectric thickness of $120\,\mu\mathrm{m}$.

This process is used to realize the following multilayer stack-up: unclad $100\,\mu\mathrm{m}$ Rogers LCP, printed silver antenna topology, printed $120\,\mu\mathrm{m}$-thick SU-8 dielectric substrate, and printed silver microstrip topology. A profilometer scan of the printed SU-8 dielectric substrate is shown in Figure 4.17. With the deposition of many layers, the printed substrate experiences effects from surface tension and drying thus creating as a result a convex-shaped profile [26]. Across the $300\,\mu\mathrm{m}$ X-span of the center of the substrate occupied by the microstrip feed line, a profile variation of $\pm\,2\,\mu\mathrm{m}$ is measured, equivalent to 3% of the substrate thickness. Images of the printed antennas are shown in Figure 4.18, including the



(a) (b) (c)

Figure 4.16: Simulation models for inkjet-printed (a) 3- and (b) 5-director Yagi-Uda antennas with (c) detail showing a multilayer microstrip-to-slotline transition.

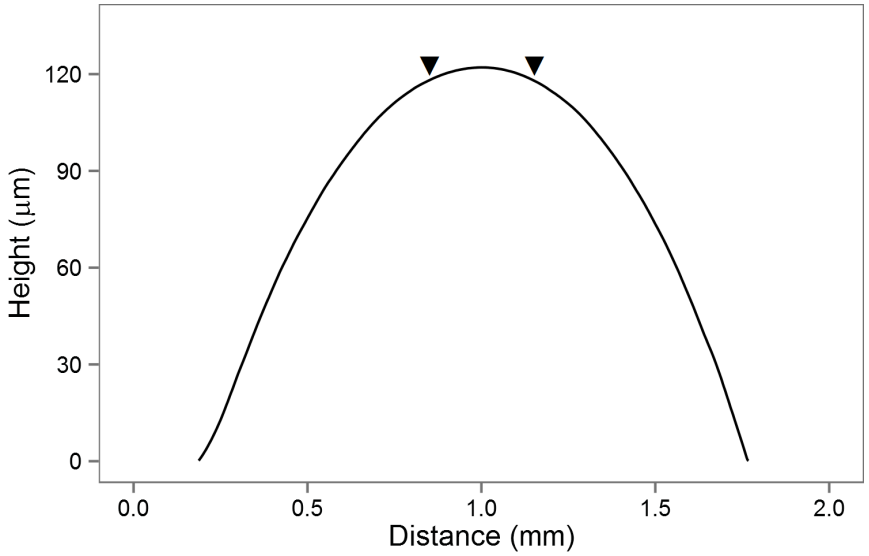


Figure 4.17: Profilometer scan of the printed 18-layer (120 µm thick) SU-8 dielectric substrate of the microstrip feedline, identifying the 300 µm area of the printed silver feedline (▼).

3- and 5-director antenna structures and detailed images of the printed dielectric substrate, driving dipole, and slight substrate bending upon end-launch connector mounting.

Upon completion of fabrication, end-launch connectors provided by Southwest Microwave are mounted onto the antennas for RF characterization. S11 return loss measure-

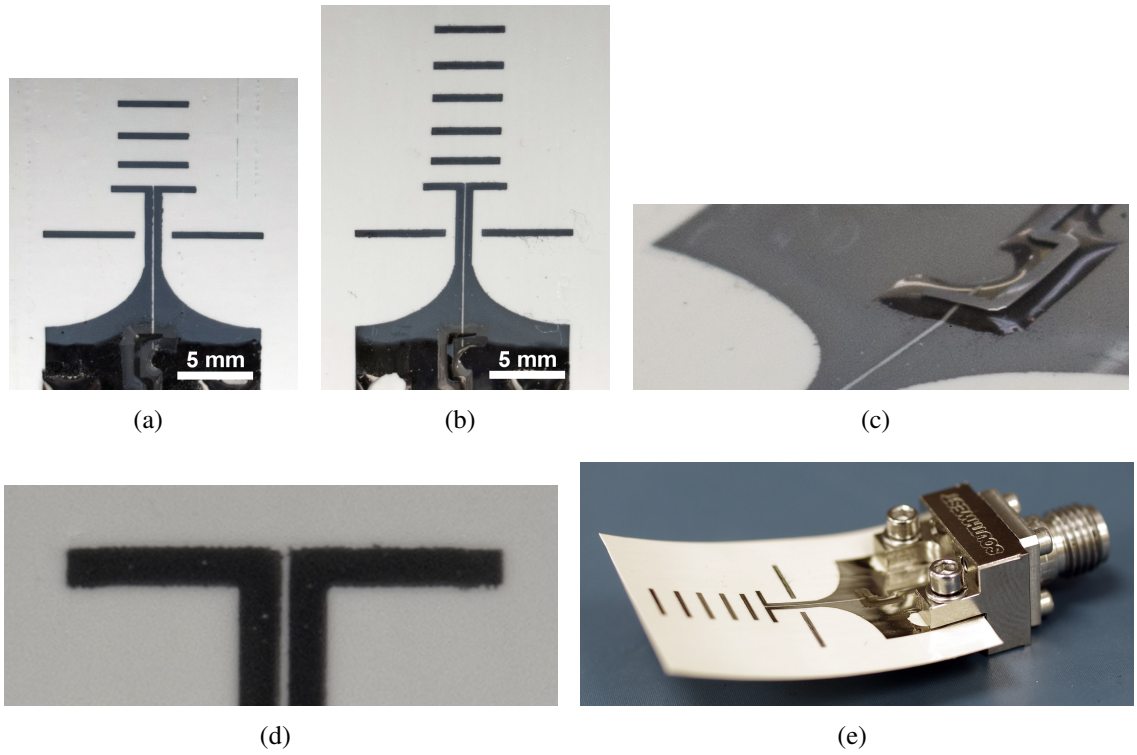


Figure 4.18: Inkjet-printed multilayer (a) 3- and (b) 5-director Yagi-Uda antennas with detail images showing (c) the printed dielectric substrate for the microstrip-to-slotline feeding transition, (d) driving dipole, and (e) slight substrate bending.

ments are then performed from 21–27 GHz using an Anritsu 37369 VNA, shown in Figure 4.19. Return loss measurements show good agreement with simulated results as well as efficient matching at 24.5 GHz, further demonstrating the integrity of both the metallic and dielectric ink materials used within the inkjet printing process.

The realized gain of the fabricated antennas is measured with a mm-wave far-field measurement system utilizing a $20\,\mathrm{dB}$ standard gain horn antenna provided by Fairview Microwave (Fairview Microwave, Allen, TX, USA) at a distance of $45\,\mathrm{cm}$. A plot of the measured and simulated end-fire realized gain for the 3 and 5-director antennas from 23–$26\,\mathrm{GHz}$ is shown in Figure 4.20. Maximum end-fire realized gains of 6 and $8\,\mathrm{dBi}$ for the 3 and 5-director designs, respectively, are achieved within the 24.5 GHz ISM band. These measurements improve upon the the $7\,\mathrm{dBi}$ realized gain of a previous effort with a Vivaldi antenna achieved in [75], demonstrating the highest-gain inkjet-printed antenna within the

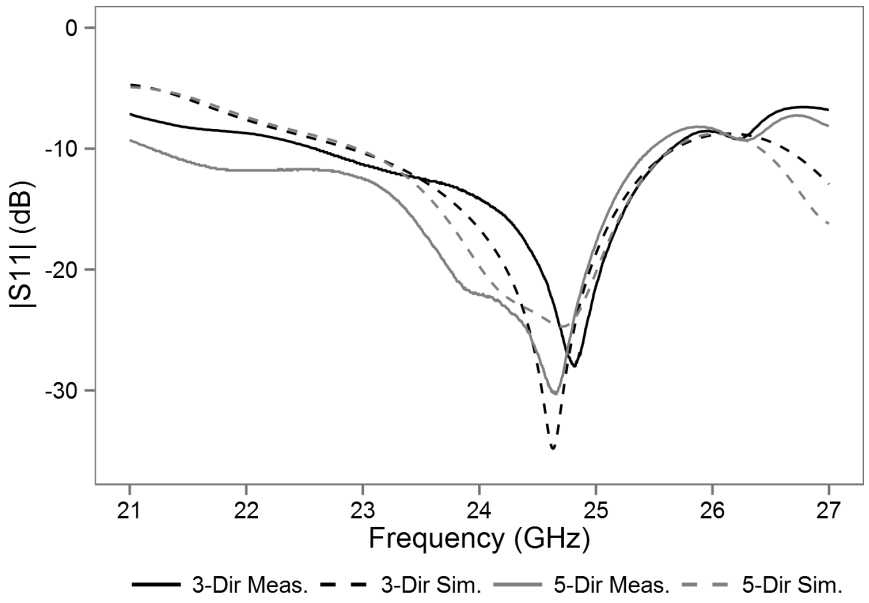
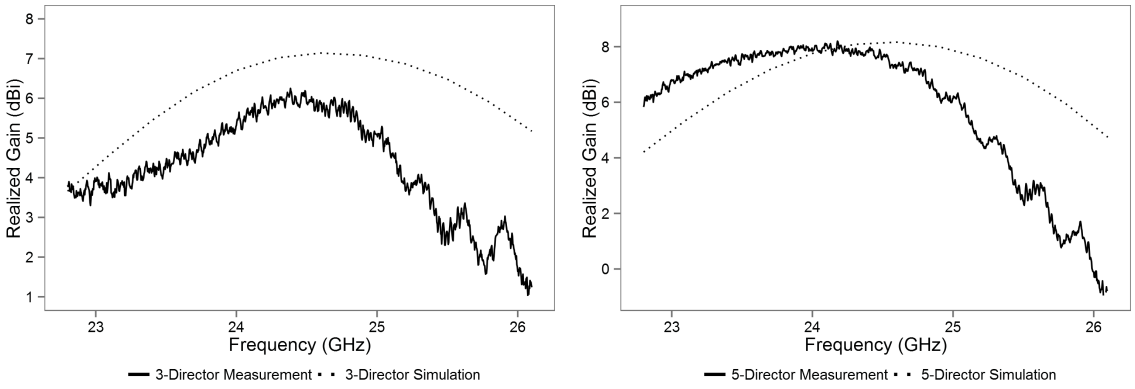


Figure 4.19: Simulated and measured return loss for the inkjet-printed 3 and 5-director Yagi-Uda antennas.

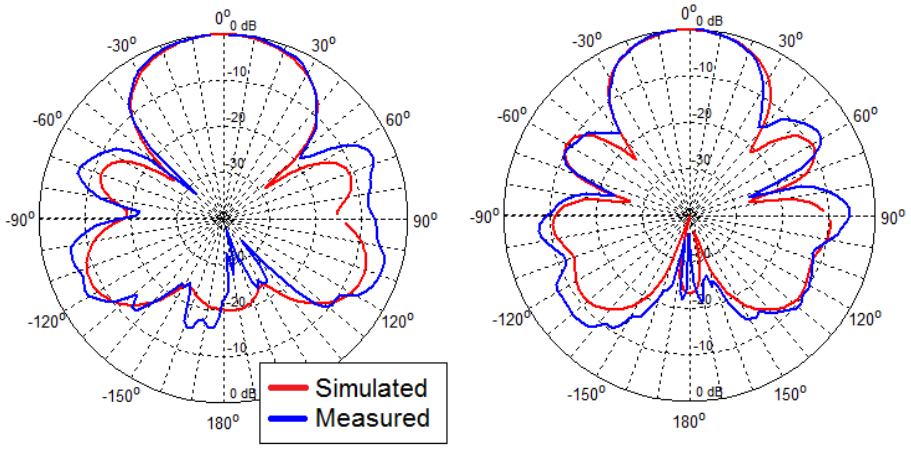


(a) (b)

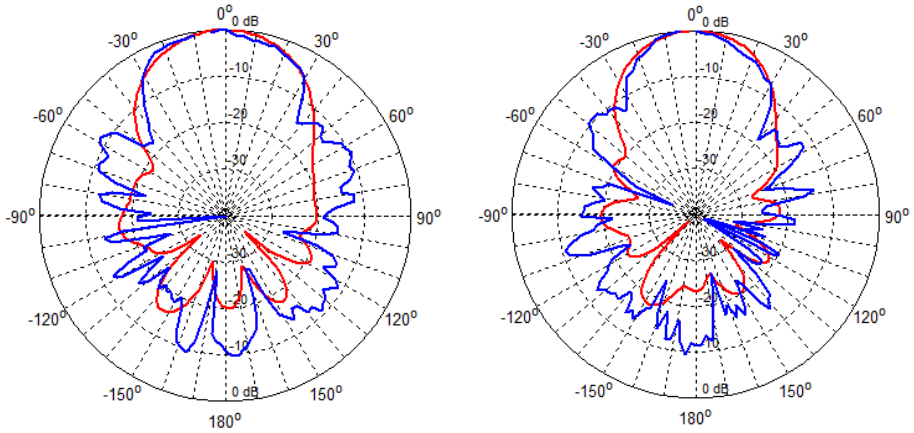
Figure 4.20: Simulated and measured realized gain for inkjet-printed (a) 3- and (b) 5-director Yagi-Uda antennas.

outlined frequency band at the time of publication. Though the measured results match well with simulated data in the lower frequencies of the measured range, discrepancies between the two in the higher frequencies are likely the result of substrate deformation during measurement as well as standing waves present in the coaxial feed-lines of the measurement system that were unable to be removed from measurements.

The radiation patterns of the printed antennas are measured using a mm-Wave far-field



(a)



(b)

Figure 4.21: Simulated and measured normalized (a) Y-Z and (b) X-Y E-field radiation patterns for inkjet-printed (left) 3- and (right) 5-director Yagi-Uda antennas.

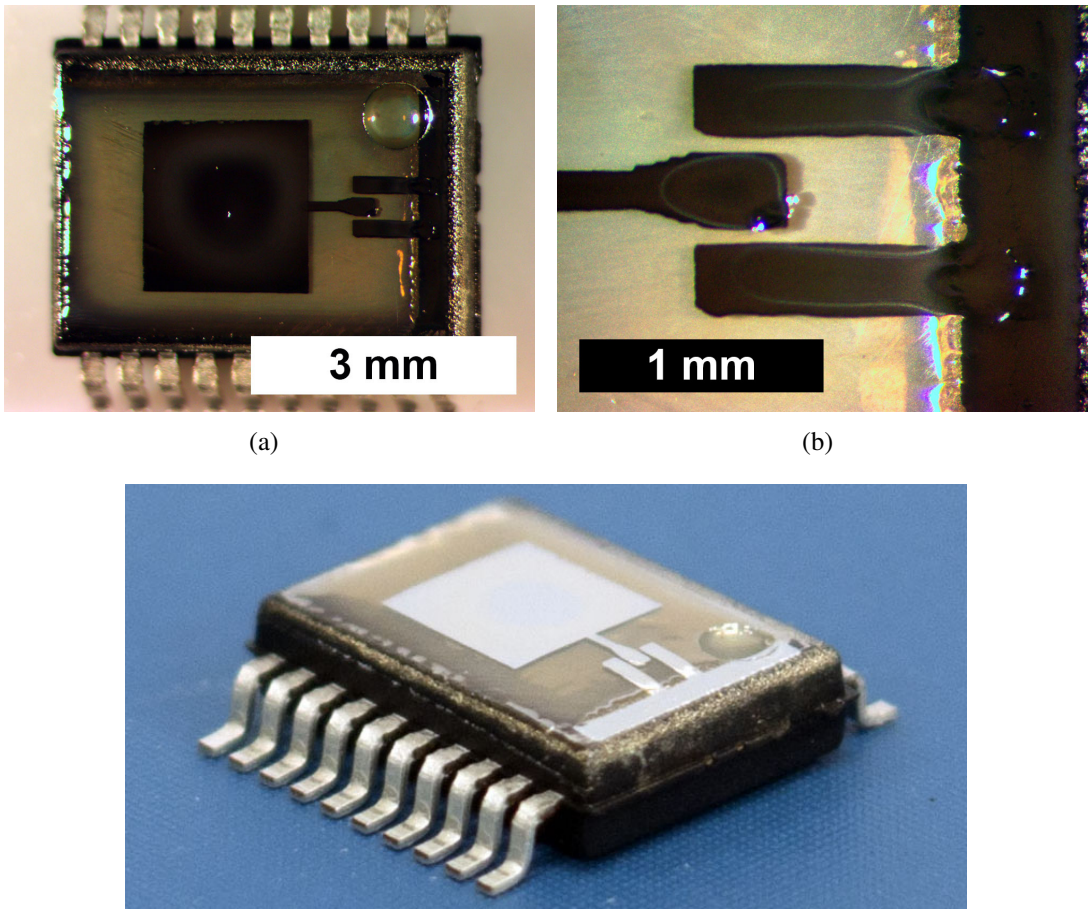
rotational measurement system setup with a $45\,\mathrm{cm}$ distance between interrogating antenna and antenna under testing. Normalized E-field radiation patterns in the X/Y (ϕ sweep) and X/Y (θ sweep) planes of the antennas are measured and compared with simulated patterns in Figure 4.21. The measured Y/Z radiation pattern cuts in Figure 4.21(a) show excellent agreement with simulations for both the 3- and 5-director designs. The measured X/Y radiation pattern cuts in Figure 4.21(b) exhibit good agreement with simulations in the end-fire $0°$ direction but experience discrepancies with slightly enlarged side-lobes, specifically in the back-side $180°$ region. These deviations are likely the result of substrate bending

during measurement, where a deformation in the X/Y plane of the antenna is conducive to a greater degree of error in the X/Y radiation pattern measurements. A second source of error could result from the modeling of the end-launch connector in simulations. Though the connectors were included in simulations, nonidealities present in the feeding structure model have the potential to affect the radial efficiency of the antenna in different directions.

4.3 SoP Patch Antenna Integration with IC Molding

With the establishment of selectively-patterned RF substrates, efforts are aimed to demonstrate inkjet printing processes for the fabrication of mm-wave on-package antenna structures to be used with package-integrated feeding methods, such as wireless die coupling and through-package vias [1, 76]. A multilayer $30\,\mathrm{GHz}$ patch antenna is fabricated on a standard IC chip package. Utilizing metallic inks for conductors and dielectric inks for thick substrates, a multilayer structure is fabricated directly onto an IC chip package and measured to verify the integrity of the injket-printed system [6].

The inkjet printing fabrication of the multilayer on-package patch antenna is a multistep process of depositing dielectric and metallic inks to create a fully-additive post-processed structure. Fabrication begins with the deposition and curing of 2 layers ($10\,\mu\mathrm{m}$) of SU-8 dielectric ink in order to provide isolation from the IC package and smoothen the rough package surface. Next, 5 layers ($2.5\,\mu\mathrm{m}$) of silver nanoparticle ink are deposited and cured to pattern the ground plane of the antenna. To pattern the thick dielectric substrate, two 7-layer printing and curing sessions of the SU-8 polymer ink are performed. The utilization of this multi-session printing scheme allows for the realization of thick dielectric patterns while maintaining an acceptable surface uniformity, avoiding the convex surface profile resulting from a single-session deposition of too much ink material [26]. Fig. 2.3 shows profile scans of the printed dielectric substrate after the first and second 7-layer sessions. After the printing and curing of the 14-layer ($120\,\mu\mathrm{m}$) dielectric substrate, 3 layers ($1.5\,\mu\mathrm{m}$) of silver nanoparticle ink are printed and cured, completing the fabrication. The inkjet-



(a) (b)

(c)

Figure 4.22: Inkjet-printed on-package 30 GHz patch antenna: (a) top view, (b) CPW feed and via detail, and (c) perspective view.

printed on-package patch antenna is shown in Fig. 4.22, including top view, perspective view, and detail of coplanar waveguide (CPW) feed and vias.

The return loss of the fabricated on-package mm-wave patch antenna is measured with an Anritsu 37369A VNA utilizing 250 µm pitch probes from Cascade Microtech. The measured and simulated return loss of the printed patch antenna is shown in Fig. 4.23. Measured results for return loss compare well to simulations, exhibiting a 0.3% deviation in resonance frequency from the simulated 30.5 GHz.

Simulated radiation pattern cuts in the Y/Z and X/Z planes are shown in Fig. 4.24, displaying a large broadside directivity typical of a square patch antenna. Realized broadside

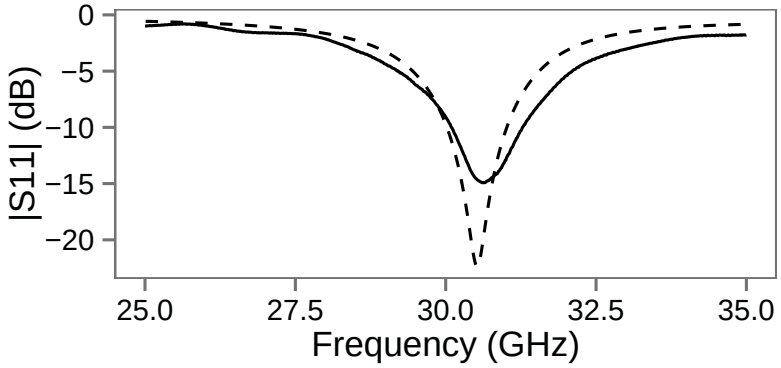
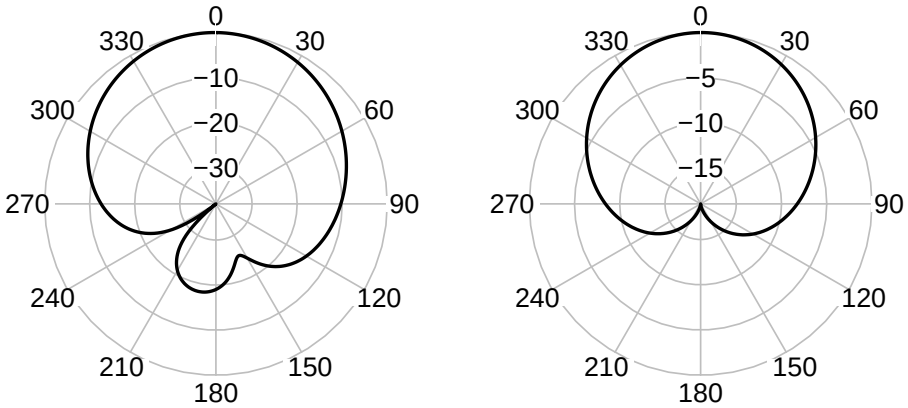


Figure 4.23: Return loss of (– –) simulated and (—) fabricated antennas.



(a) (b)

Figure 4.24: Simulated (a) Y/Z and (b) X/Z normalized radiation pattern cuts.

(+Z) gain is found in simulation to reach $1\,\mathrm{dB}$, where efficiency is affected by the CPW-to-microstrip feed transition and the CPW vias to ground required for probe measurement.

CHAPTER 5

FULLY-PRINTED FIRST-LEVEL INTERCONNECTS FOR MMIC DEVICES

Three-dimensions (3D) first-level interconnects are required in order to interface an IC die with a packaging substrate and other electronic components within the same package. The two most popular methods of realizing these interconnections are wire bonding and flip-chip techniques. As discussed in Chapter 3, wire bonding is a relatively cheap and rapid interconnection option, yet it is often prone to sway upon molding and high parasitic inductance, often requiring passive components for compensation at mm-wave frequencies [1]. Flip-chip techniques reduce interconnection length and parasitics yet suffer from high sensitivity to coefficient of thermal expansion (CTE) mismatch as well as detuning from the close proximity to on-package signal routing below the IC [2].

This chapter outlines the development and implementation of fully-printed 3D first-level interconnects for mm-Wave MMIC devices. Two first-of-their-kind inkjet-printed interconnection configurations are explored to address popular bare-die assembly schemes, including surface mount and cavity-embedded architectures [7, 77, 8]. 2D cross-section schematics of the two assembly configurations are shown in Fig. 5.1. For the first approach in Fig. 5.1(a), the MMIC die is mounted onto the surface of a packaging substrate where inkjet printing is used to pattern 3D dielectric ramps and then metallic traces to interconnect between the packaging substrate and the pads on the surface of the die. With the second configuration in Fig. 5.1(b), a MMIC die is mounted within a cavity in the packaging substrate where inkjet printing is used to pattern a dielectric fill into the gaps between the die and the packaging substrate along with metallic traces interconnecting the pads on the surface of the die with the packaging substrate. Both configurations are commonly used within industry, where the surface mount approach provides a simpler assembly with respect to the packaging substrate stack-up while cavity-embedding typically enables a

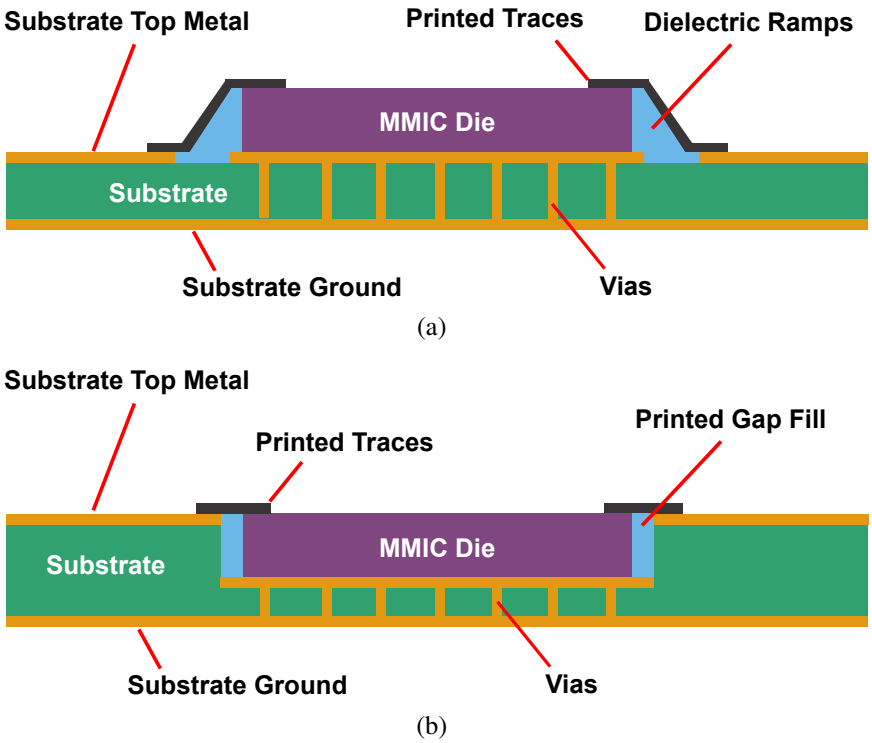


Figure 5.1: 2D cross-section schematics for two assembly configurations with printed first-level interconnects: (a) surface mount with printed ramp interconnects and (b) cavity-embedded with printed cavity transitions.

shorter interconnect length due to the planarity of the die with the substrate. In contrast to traditional techniques, inkjet printing allows for the miniaturization of interconnect parasitic losses through the patterning of conformal, low-profile RF transitions with reduced insertion loss and improved matching between SiP components.

These additive approaches require an extensive characterization of ink materials used within the inkjet printing procedure, specifically the interaction of dielectric and metallic inks to achieve the desired 3D interconnect features through a layer-by-layer fabrication process. Additionally, careful consideration must be placed on integrating the proposed inkjet-printed transitions with practical MMIC dies, including such parameters as pad width, pad pitch, and die thickness. RF characterization of the proposed interconnects is presented with active MMIC dies in order to evaluate the loss of the transitions and understand their effect on a broader system level, targeting such parameters as input/output

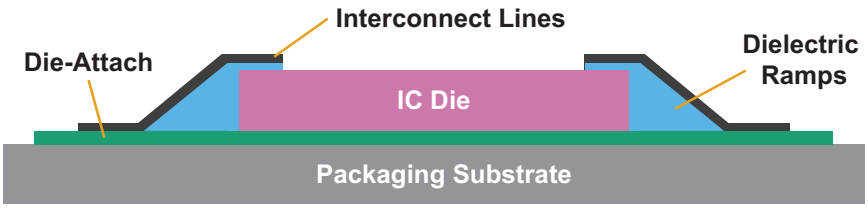


Figure 5.2: Cross-section of proposed inkjet-printed 3D interconnects.

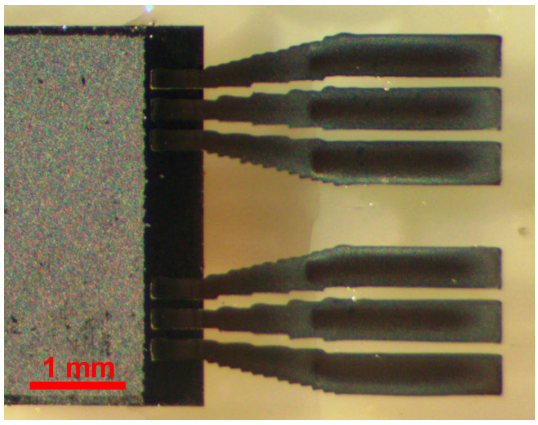
matching and gain. Quantitative comparisons with traditional bonding techniques, including wire and ribbon bonding, is targeted in order to provide an apples-to-apples comparison between the proposed printing methods with the current state-of-the-art.

5.1 3D Ramped Interconnects for Surface Mount IC Packaging

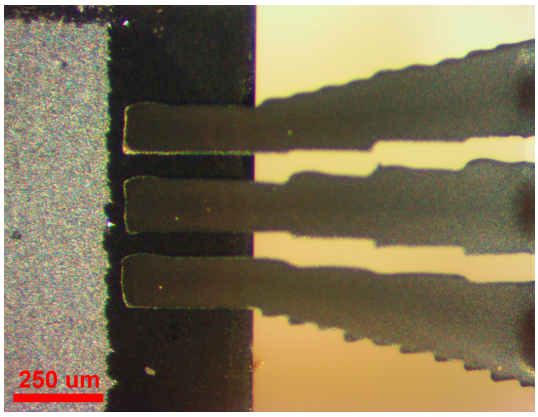
In order to assess the current challenges of cost and versatility in wireless mm-wave SiP solutions, this section outlines the development of 3D interconnects for surface-mount assembly configurations using inkjet printing. Coplanar waveguide (CPW) transmission lines are fabricated and measured to interconnect a silicon die with a packaging substrate using conductive silver nanoparticle and dielectric polymer inks as a first-of-its-kind proof of concept [7]. These fully printed interconnects are then used to integrate a die with a mm-wave bow-tie slot antenna to demonstrate the feasibility of realizing low cost, robust SiP wireless systems.

5.1.1 Fully-Printed Ramp Interconnects

The design of the 3D interconnects is composed of the following elements shown in Fig. 5.2: an IC die, a packaging substrate, a die attach material, a dielectric ramp structure, and CPW transmission lines. For this work, a blank $2 \times 2.7\,\mathrm{mm}$ silicon die with a thickness of $50\,\mu\mathrm{m}$ and a bulk resistivity of 10 ohm-cm is used as a proof-of-concept prototype for mm-Wave transceiver dies. The packaging substrate is chosen to be a 1 mm thick glass slide in order to facilitate handling throughout the fabrication process, however this technology could be applied to other packaging substrates, such as metallic, flexible organic, and ceramic. A



(a)



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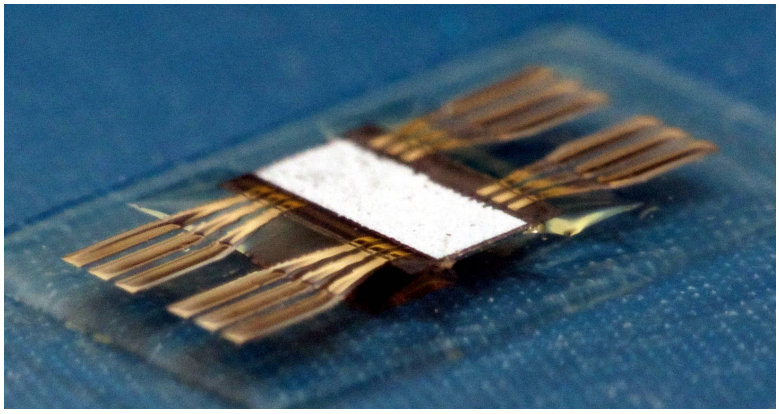


(c)

Figure 5.3: (a–b) Micrographs and (c) perspective image of the inkjet-printed CPW interconnect samples.

die-attach material is used to adhere the silicon die to the glass packaging substrate. In order to create a three-dimensional transition between the top of the die and the substrate below, ramp structures are also required to transition the $50\,\mu\mathrm{m}$ thickness of the die. $50\,\Omega$ CPW transmission lines are employed with a fan-out structure to provide interconnection and maintain the desired impedance considering the transition of ϵ_r between the die (ϵ_r = 11.9) and the substrate (ϵ_r = 4.82).

Fabrication of the 3D interconnect samples begins with the patterning of the die attach material on a bare glass slide using a Dimatix DMP-2831 piezoelectric inkjet materials printer. Three layers of the SU-8 polymer ink are printed and then baked with a 60–120° ramp over $10\,\mathrm{min}$. A silicon die is then manually placed onto the die attach, followed by

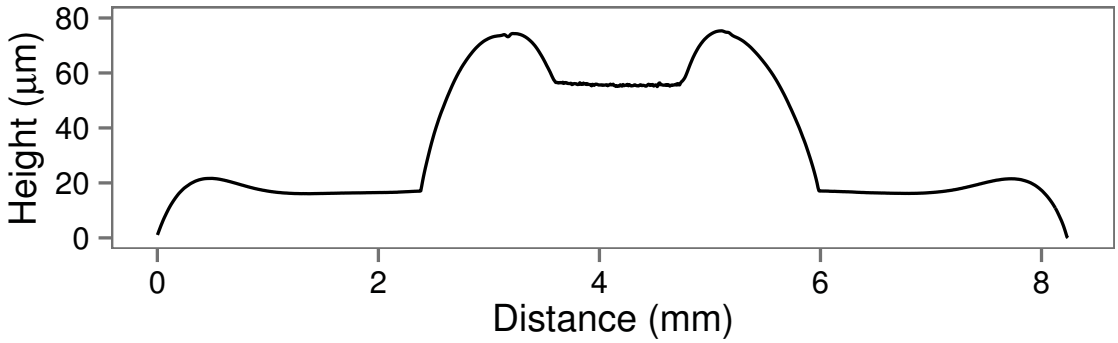


Figure 5.4: Profilometer scan of the inkjet-printed 3D interconnect sample, including: die attach, ramp structures, and silicon die.

the remainder of the SU-8 ink curing profile: a $250\,\mathrm{mJ/cm^2}$ exposure of $365\,\mathrm{nm}$ ultraviolet (UV) light and a $100°$ bake for $7\,\mathrm{min}$. For this demonstration, the die attach is acting as an adhesion layer for both the die and the printed interconnects on the packaging substrate.

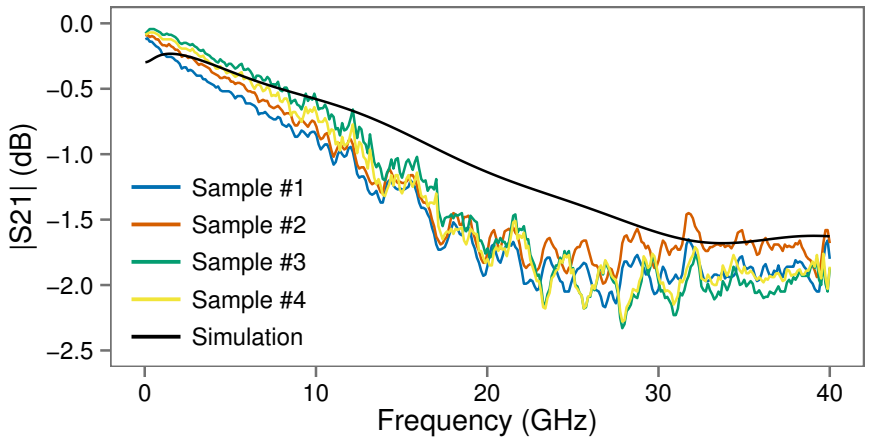
With the die attached, dielectric ramps are printed to transition between the die and the substrate. The ramp structures are patterned to extend approximately $400\,\mu\mathrm{m}$ onto the surface of the die and $800\,\mu\mathrm{m}$ onto the substrate. The purpose of extending the pattern onto the surface of the die is to allow for a uniform ramp to be realized with the minimum amount of printed layers, where adhesion of the ramp to the top of the die is expedited when material is deposited onto both the the die and the substrate instead of the substrate alone due to the rheological nature of the polymer ink. Additionally, the extension of the material onto the die allows for increased adhesion of the printed interconnects to the unpolished surface of the die. Five layers of the SU-8 polymer ink are printed to pattern the ramps, followed by the previously outlined curing profile with the substitution of a $300\,\mathrm{mJ/cm^2}$ UV light exposure to account for the thicker dielectric ramps.

Fabrication is concluded with the printing of the CPW transmission line traces. Before printing, the sample undergoes a $30\,\mathrm{s}$ exposure to UV ozone (O_3) to optimize the surface energy of the printed ramps and substrate for the wetting of the CCI-300 ink. Three layers of the silver nanoparticle ink are printed, followed by oven sintering at $180°$ for $1\,\mathrm{h}$.

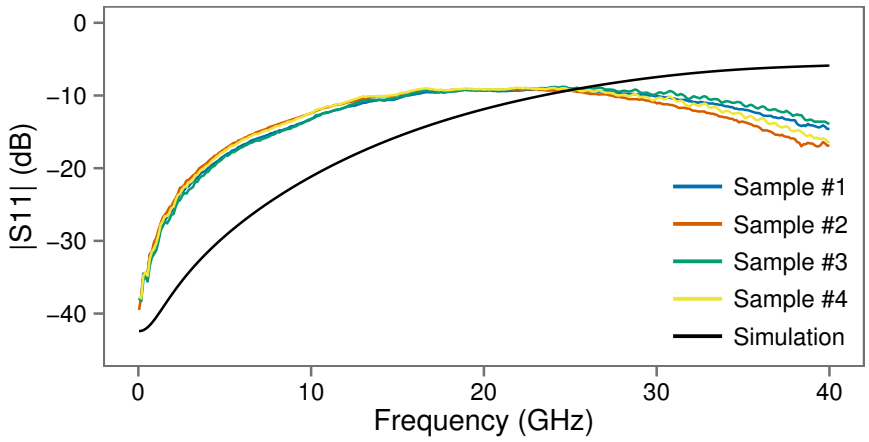
Images of the printed 3D CPW interconnect samples are shown in Fig. 5.3. The stag-

gering effect present in the fan-out of the traces is due to the $20\,\mu\mathrm{m}$ resolution of the CPW line pattern. The key dimensions of the printed CPW interconnects exhibit on average less than $\pm\ 3\%$ variation across the four printed samples. A profilometer scan is presented in Fig. 5.4, detailing the height of the printed die attach, ramp structures, and silicon die. The height of the three-layer die attach is measured to be $16\,\mu\mathrm{m}$ and exhibits good uniformity across the center of the film where the die is placed. The maximum height of the five-layer ramp structures reaches up to $20\,\mu\mathrm{m}$ above the die attach due to the presence of printed material on the surface of the die as well as the natural tendency of the SU-8 polymer ink to form a convex profile when a high density of material is printed in a limited area. The surface of the $50\,\mu\mathrm{m}$ die is measured to be $40\,\mu\mathrm{m}$ above the die attach, determining that the die recesses approximately $10\,\mu\mathrm{m}$ into the die attach under the outlined processing conditions.

High frequency simulations of the CPW interconnect prototypes are conducted using CST Microwave Studio. The S-parameters of the printed interconnect samples are measured with an Anritsu 37369A VNA utilizing $250\,\mu\mathrm{m}$ pitch ground-signal-ground (GSG) probes from Cascade Microtech. Insertion and return loss parameters include the interaction of three general forms of loss in a standard transmission line: dielectric loss, conductive loss, and radiated loss. Measured and simulated insertion loss parameters from 0.4–$40\,\mathrm{GHz}$ are presented in Fig. 5.5(a). The measured results of the printed samples show excellent consistency with each other, however discrepancies less than $1.5\,\mathrm{dB}$ in magnitude are witnessed throughout the band. Deviations from the simulation values are likely the result of the morphology of the dielectric ramp structures, a feature that is difficult to precisely model in simulation. Fig. 5.5(b) presents the measured and simulated return loss parameters over the same frequency range. As with the insertion loss measurements, excellent consistency between the printed samples is demonstrated. Deviation from simulated return loss is likely the result of imperfections present in the 3D modeling of the GSG probes used for measurement.



(a)

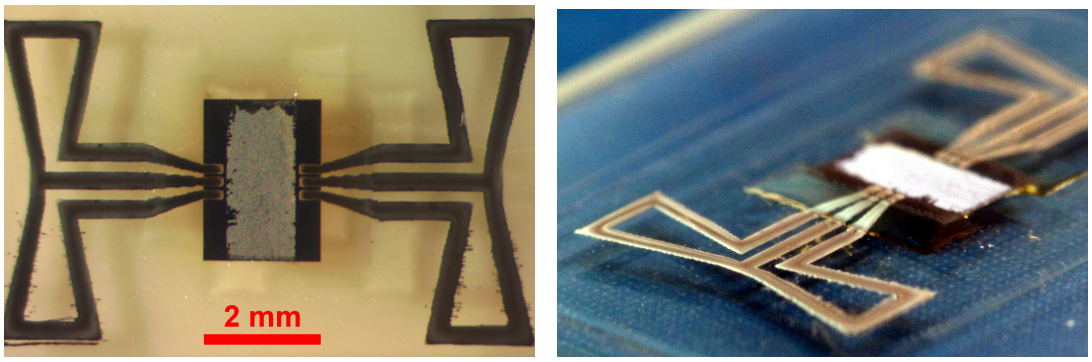


(b)

Figure 5.5: (a) Insertion and (b) return loss simulations and measurements for the inkjet-printed first level CPW interconnects.

5.1.2 Integration with SiP Bow-Tie Antenna

In order to demonstrate the effectiveness and versatility of entirely inkjet-printed 3D interconnects as SoP applications, integration with a mm-wave antenna is presented. A bow-tie slot antenna is chosen in order to preserve the efficiency of the CPW feed line interconnect from the die. The bow-tie slot antenna offers a simple planar design along with a wide operational bandwidth suitable for mm-wave wireless technologies. The antenna is designed to operate beyond the 24.5 GHz ISM band using a miniaturized wideband bow-tie slot configuration. This frequency range is also suitable for probe station measurement where the metallic chuck acts as a reflector to antenna on the glass packaging substrate, which has an



(a) (b)

Figure 5.6: (a) Micrograph and (b) perspective image of the inkjet-printed on-package mm-wave bow-tie antenna samples.

approximate electrical thickness of $\lambda/4$ around $30\,\mathrm{GHz}$.

The fabrication of the antenna samples is identical to that of the inkjet-printed CPW interconnects previously outlined. Images of the printed mm-wave bow-tie antenna samples that are connected to the IC through the proposed inkjet-printed 3D interconnects are presented in Fig. 5.6. With the exception of several minor instances of nozzle failure during printing, the printed samples exhibit good consistency with each other and the intended design pattern.

Return loss measurements of the printed antennas are recorded to verify the effectiveness of the presented 3D interconnect method for mm-wave wireless systems. Fig. 5.7 presents the measured and simulated return loss parameters of the two printed antenna samples over the range of 20–40 GHz. The measured return loss of the printed samples exhibits resonance within and beyond 24.5 GHz ISM band. Deviations from the simulated return loss are likely the result of the presence of the GSG probes used for measurement, as well as the morphology of the SU-8 ramps previously discussed. Farfield simulations of the bow-tie antenna yield a radiation efficiency of 51% and a realized gain of 6.3 dB in the endfire direction away from the die and 1.6 dB in the broadside direction at 30 GHz. Radiation efficiency has the potential to be increased through the investigation of lower-loss dielectric ink formulations for the printed die attach and packaging substrate structures.

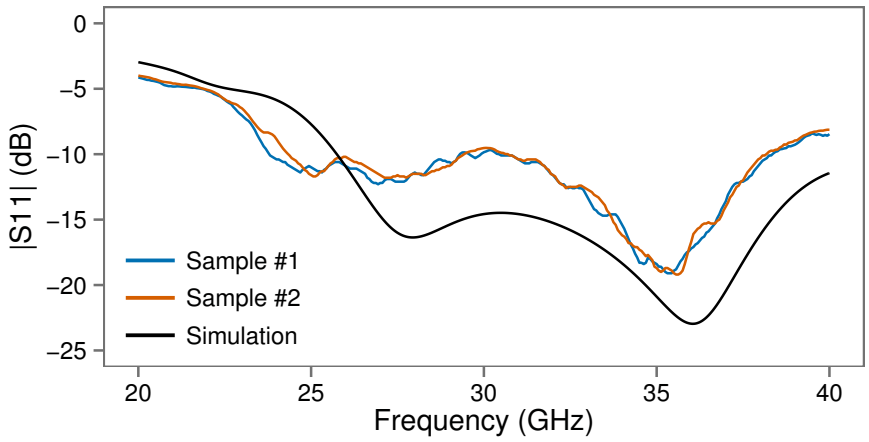


Figure 5.7: Return loss simulations and measurements for the printed mm-wave bow-tie slot antennas.

5.2 Printed Ramps with Surface Mount Ka-Band MMIC Devices

The further development of printed ramp-based interconnects allows for the integration of mm-wave MMIC devices on virtually any host substrate, removing the need for milling or designing a substrate around a recessed cavity. This section outlines for the first time the development of fully inkjet-printed mm-wave 3D ramp interconnects for Ka-band active wireless devices at the discrete IC level for wireless mm-wave multi-chip module (MCM) packaging solutions [77]. An inkjet printing process is outlined utilizing conductive and dielectric inks to realize printed RF and DC interconnects for MMIC dies, including a $0\,\mathrm{dB}$ attenuator for verification and a Ka-band low-noise amplifier (LNA) for further evaluation.

5.2.1 Integration with Ka-Band Attenuator MMIC

As an initial demonstration, a TriQuint TGL4201-00 GaAs $0\,\mathrm{dB}$ attenuator is chosen to evaluate the feasibility of inkjet printing ramp interconnects to Ka-Band MMICs. The $500 \times 500 \times 100\,\mu\mathrm{m}$ TGL4201-00 essentially acts as an RF *through* and exhibits an insertion loss of approximately 0–$0.2\,\mathrm{dB}$ from DC–$30\,\mathrm{GHz}$ and a return loss of approximately $15\,\mathrm{dB}$ from DC–$40\,\mathrm{GHz}$. Bare die measurements for the TGL4201-00 are not included in this work do to its listed specifications and the sensitivity limitations of the measurement

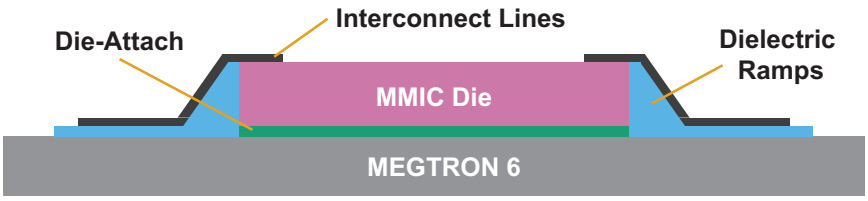


Figure 5.8: 2D cross-section schematic of inkjet-printed ramp interconnects for a MMIC die on a MEG6 substrate.

equipment used.

A 2D cross-section schematic of the printed ramp stack-up is shown in Fig. 5.8. First, a die attach is printed onto a Panasonic MEGTRON6 (MEG6) substrate with 1 layer of SU-8 ink. After the die is placed, the curing profile outlined in Section II is performed with a $300\,\mathrm{mJ/cm^2}$ UV exposure. Once attached, 4 layers of SU-8 ink are printed and cured with a $400\,\mathrm{mJ/cm^2}$ UV exposure to deposit ramps interfacing the MEG6 with the top of the attenuator die, where the pattern of the ramp is chosen to overlap $40\,\mu\mathrm{m}$ onto the die to ensure ramp connectivity to the top of the die. The SU-8 pattern also behaves as an adhesion film to promote the subsequent metallic patterning on the MEG6 substrate. The sample then undergoes a $2.5\,\mathrm{min}$ UV-O_3 treatment to ensure proper wetting of the silver nanoparticle (SNP) ink on the printed ramps. Finally, coplanar waveguide (CPW) interconnects are patterned with 4 layers of SNP and then thermally sintered as outlined in Section II. Fig 5.9 shows a micrograph of the TGL4201-00 die with printed ramp interconnects. The maximum slope of the printed dielectric ramps is measured to reach approximately $35°$, which has been demonstrated as a suitable slope for multilayer inkjet printing [64].

As seen in Fig. 5.9, a taper is included in the printed CPW interconnects to transition from the $15\,\mu\mathrm{m}$ pitch of the RF pads on the die to a $250\,\mu\mathrm{m}$ pitch to faciliate measurement. The interconnected attenuator sample is measured from 10–$40\,\mathrm{GHz}$ using an Anritsu 37369A VNA with Cascade Microtech ACP40-GSG-250 probes. Measured S-parameters of the interconnected device are shown in Fig. 5.10. The insertion loss of two back-to-back printed ramp interconnects with the attenuator die is measured to be $1.08\,\mathrm{dB}$ at $24.5\,\mathrm{GHz}$, yielding an insertion loss of approximately $0.5\,\mathrm{dB}$ per ramp interconnect, or approximately

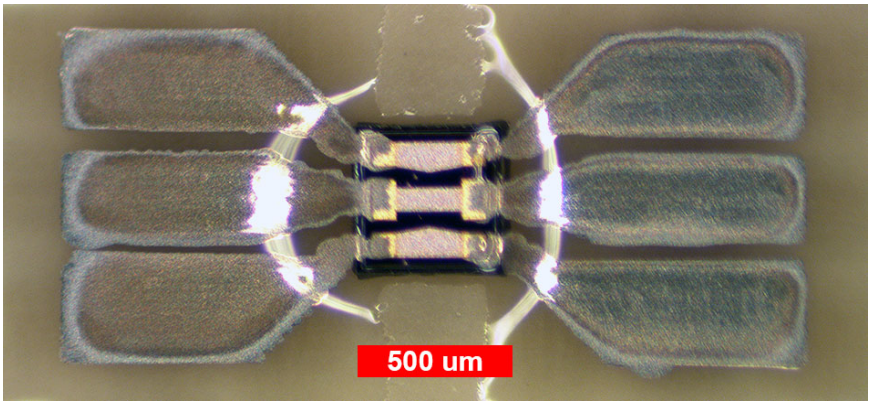


Figure 5.9: Inkjet-printed ramp interconnects interfacing a Ka-band GaAs attenuator die.

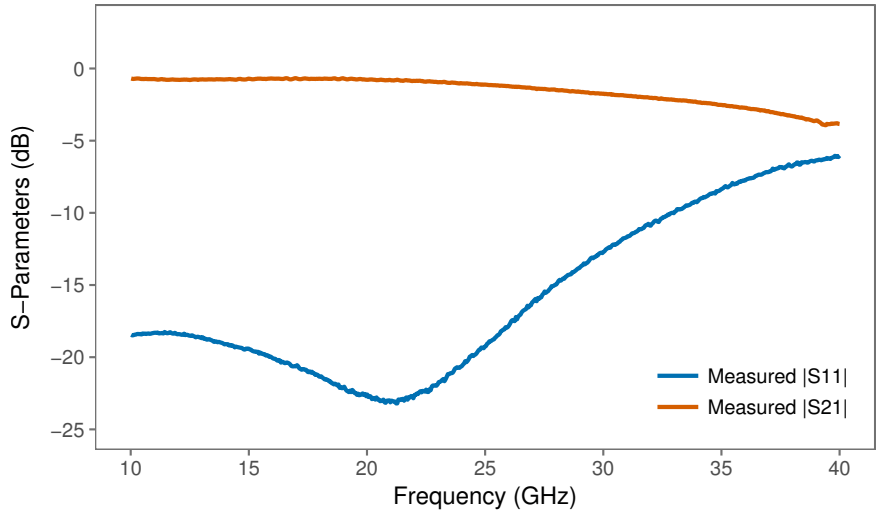
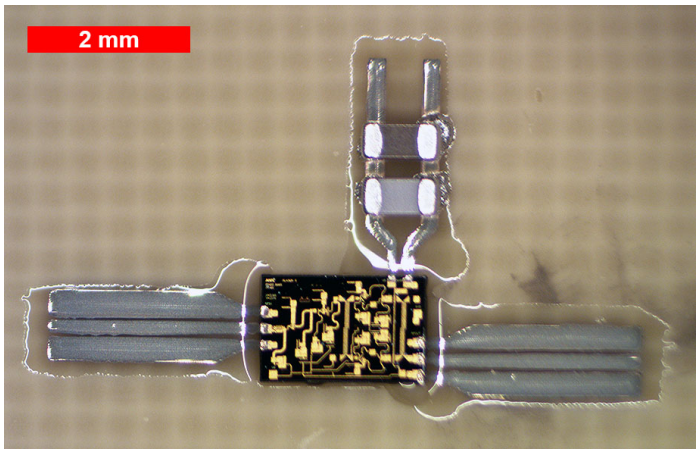


Figure 5.10: Measured S-parameters for back-to-back inkjet-printed ramp interconnects with a $0\,\mathrm{dB}$ GaAs attenuator die on a MEG6 laminate.

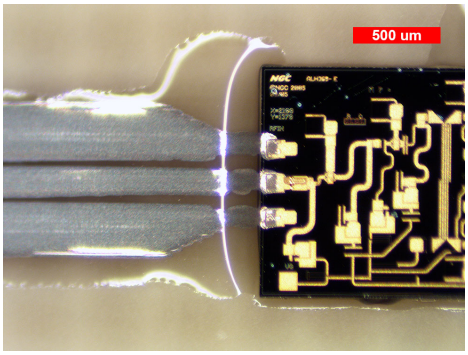
$0.45\,\mathrm{dB/mm}$ for a single interconnect. The return loss is measured to be to be greater than $10\,\mathrm{dB}$ up to $33\,\mathrm{GHz}$, demonstrating adequate matching throughout the bottom half of the Ka-band where further improvements can be achieved through the optimization of the 250–$150\,\mu\mathrm{m}$ pitch CPW taper dimensions.

5.2.2 Integration with Ka-Band LNA MMIC

With the process of printed ramp interconnection verified with an attenuator die in Section III, focus is shifted to the integration with active devices in the Ka-band. A Hittite HMC-ALH369 GaAs high-electron-mobility transfer (HEMT) MMIC LNA is chosen for



(a)



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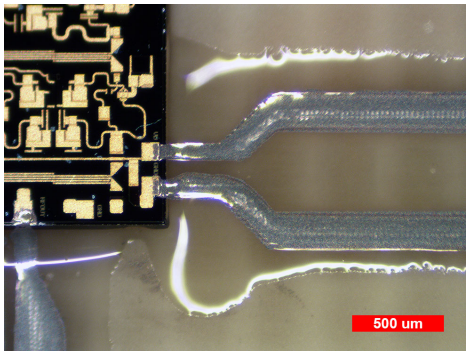


(c)

Figure 5.11: Inkjet-printed RF and DC ramp interconnects interfacing a Ka-band GaAs HEMT LNA MMIC on a MEG6 laminate: (a) full device, (b) RF input detail, (c) DC bias detail.

the evaluation of these printed ramp interconnects, exhibiting a nominal gain of $22\,\mathrm{dB}$ over the range of 24–$40\,\mathrm{GHz}$. In addition to the two RF input/output ports of the die, interconnects must also be printed at the Vdd and GND pads with the inclusion of bypass capacitors to ensure proper biasing.

The fabrication process begins with the attaching of the $2.10 \times 1.37 \times 0.10\,\mathrm{mm}$ HMC-ALH369 MMIC, where 2 layers of SU-8 ink are printed as a die attach and cured. Next, 5 layers of SU-8 ink are inkjet-printed and cured to form dielectric ramps from the MEG6 to the top surface of the LNA die as well as an adhesion film for metallic patterning. After a $2.75\,\mathrm{min}$ UV-O_3 exposure, tapered RF and DC interconnects are patterned with 6 layers of SNP ink which are then thermally sintered. As a final step, $100\,\mathrm{pF}$ and $0.1\,\mu\mathrm{F}$ 0402-

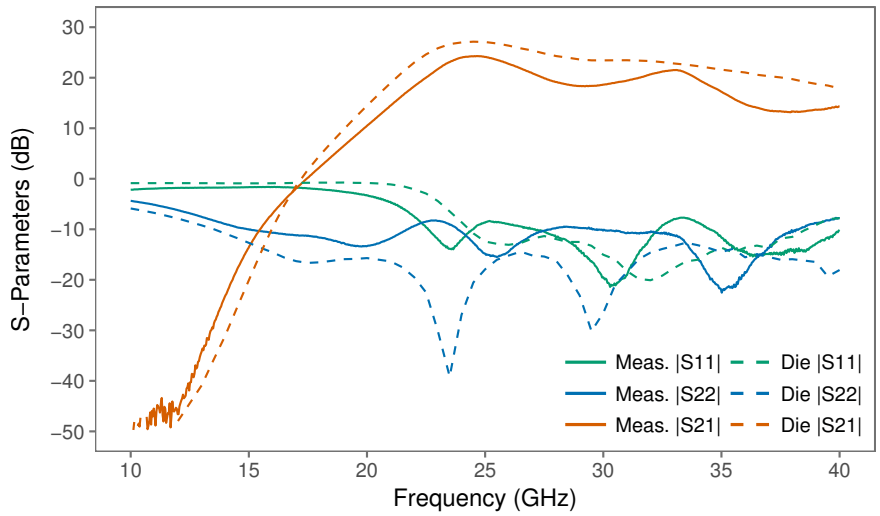


Figure 5.12: Measured S-parameters for inkjet-printed ramp interconnects with a Ka-band LNA MMIC on a MEG6 laminate compared with bare die probing.

size surface mount capacitors are placed using conductive silver epoxy to behave as bypass capacitors for the Vdd and GND lines. Fig. 5.11 shows a micrograph of the LNA MMIC with printed RF and DC interconnects, including bypass capacitors. The first $100\,\mathrm{pF}$ capacitor is located approximately $700\,\mu\mathrm{m}$ from the DC pads on the die, staying within the recommended specification of a maximum $750\,\mu\mathrm{m}$ distance.

The LNA MMIC with fully inkjet-printed ramp interconnects is measured from 10–$40\,\mathrm{GHz}$ with a $5\,\mathrm{V}$ DC bias and $-20\,\mathrm{dBm}$ input power. The measured S-parameters of the device including the printed interconnects along with bare die comparison are shown in Fig. 5.12. The gain of the device with printed interconnects is measured to be $24.2\,\mathrm{dB}$ at $24.5\,\mathrm{GHz}$. Comparing with the specification of $27.1\,\mathrm{dB}$ gain at $24.5\,\mathrm{GHz}$ for the case of a bare un-packaged die, the insertion loss of the printed ramp interconnects can be observed to be approximately $1.5\,\mathrm{dB}$ per interconnect, or $0.57\,\mathrm{dB/mm}$ at $24.5\,\mathrm{GHz}$, demonstrating a very effective low-loss interconnect to a Ka-band LNA through the use of multi-material inkjet printing.

5.3 Low Profile Interconnects for Cavity-Embedded MMIC Packaging

Cavity embedding MMICs is a popular practice in the fabrication of packaged microwave components. As shown in Fig. 5.13(a), interconnection with cavity-embedded devices is typically achieved with wire or ribbon bond transitions between a packaging substrate and the MMIC device. The planarity and length of these RF transitions are crucial parameters for determining the resulting inductance and thus any potential impedance mismatches acquired. A simple expression for the estimation of wirebond inductance in a cavity-embedded assembly is given by [78]:

$$L' = \frac{L}{l} = 20^{-7} \frac{\mathrm{H}}{\mathrm{m}} \ln\left(\frac{4h}{d}\right) \tag{5.1}$$

Equation 5.1 estimates the inductance per unit length of a wirebond over a ground plane, where h is the height above the ground plane and d is the wire diameter. It is apparent from this expression that reducing h and increasing d will effectively reduce inductance and thus improve signal transmission.

The conformal nature of inkjet printing allows for the patterning of low-profile interconnects between a packaging substrate and MMIC die in a cavity-embedded assembly scenario. Fig. 5.13(b) shows a conceptual 2D schematic of an inkjet-printed interconnect solution, which requires the deposition of an insulating dielectric gap fill as well as a conductive bridge-like transition. This section outlines the fabrication processes required for achieving these interconnects, including the gap fill process and transition patterning [8]. This additive approach is compared to a traditional ribbon bond approach through the interconnection of a Ka-band LNA, where gain and input/output matching are evaluated as performance metrics of the first-level interconnects. Finally, a Ka-band MCM front end is developed with fully-printed interconnects in order to further demonstrate capabilities with system-level integration.

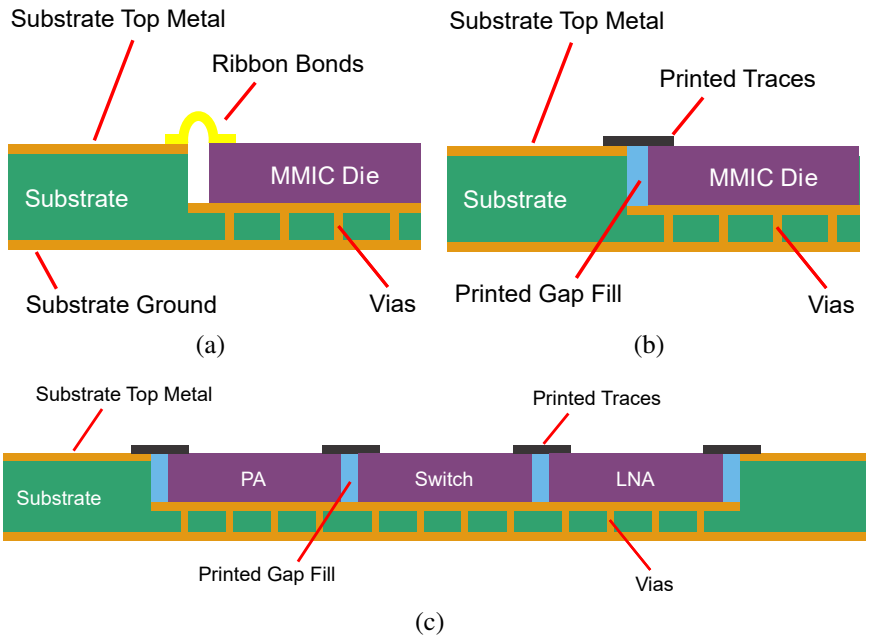


Figure 5.13: Side-view schematics summary of the printed gap filled interconnect topologies discussed in this paper. (a)-(b) Ribbon bonded LNA MMIC comparison with a inkjet printed LNA MMIC. (c) Fully inkjet printed interconnected RF front end MCM.

5.3.1 Gap Filling and Interconnection Process

A major challenge in achieving these printed transitions is choosing the materials and the correct printing processes to achieve a smooth gap fill absent of non-planar discontinuities. Solvent-based dielectric inks exhibit volume loss during curing, meaning that the height of the dielectric is difficult to predict, which can then leads to discontinuities and unconnected interconnects. SU-8 was used as the gap filling dielectric material due to high solids content and thus abilitiy to be inkjet printed at high volumes with relatively low volume loss. A rigorous evaluation of the SU-8 gap fill was performed to observe the correct amount of SU-8 to print to get a smooth transition. It was observed that 8 layers of SU-8 were needed at $15\,\mu\mathrm{m}$ drop spacing, equivalent to 1693 drops-per-inch with $10\,\mathrm{pL}$ volume size per ink droplet, to fill a gap with $100\,\mu\mathrm{m}$ depth. Fig. 5.14 shows a profilometer scan of the cavity gap before and after gap filling, demonstrating that the printed SU-8 forms a smooth transition from the substrate to the edge of the die. The SU-8 ink was printed at a $60\,^{\circ}\mathrm{C}$ stage

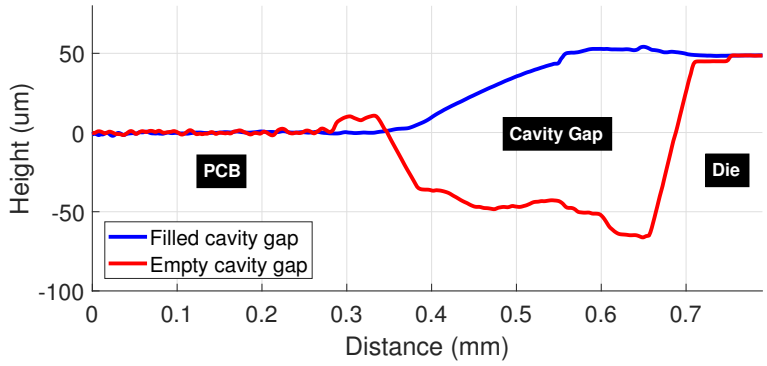
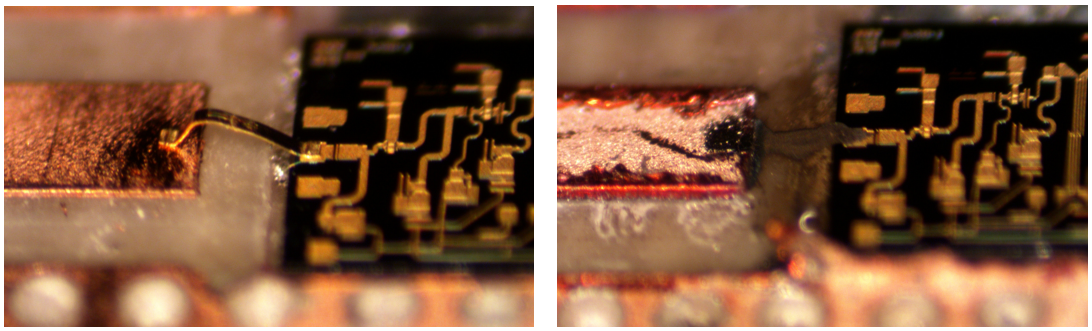


Figure 5.14: Profilometer scan of the transition area from evaluation board to chip. The red line shows the profile pre gap filling, and the solid blue is post gap filling. The post gap fill shows a smooth transition from the PCB to die edge.

temperature, followed by a UV cross-linking exposure of $500\,\mathrm{mJ/cm^2}$ and a hard bake at $155\,^{\circ}\mathrm{C}$ for $30\,\mathrm{min}$. Finally 3 layers of EMD5730 SNP ink were printed at $20\,\mu\mathrm{m}$ drop spacing, yielding a metal thickness of approximately $5\,\mu\mathrm{m}$, to pattern conductive interconnects between the packaging substrate and MMIC. The SNP ink was then sintered at $150\,^{\circ}\mathrm{C}$ for $30\,\mathrm{min}$ to complete the process.

5.3.2 Comparing Printed and Bonded Interconnects with Ka-Band LNA

To evaluate the performance of the inkjet-printed interconnect technology in a practical RF assembly, the printed gap filling interconnection process is demonstrated with an HMC-



(a) (b)

Figure 5.15: Proof-of-concept prototype images of the cavity-embedded LNA MMIC with (a) ribbon bonds and (b) printed interconnects at the RF input, respectively.

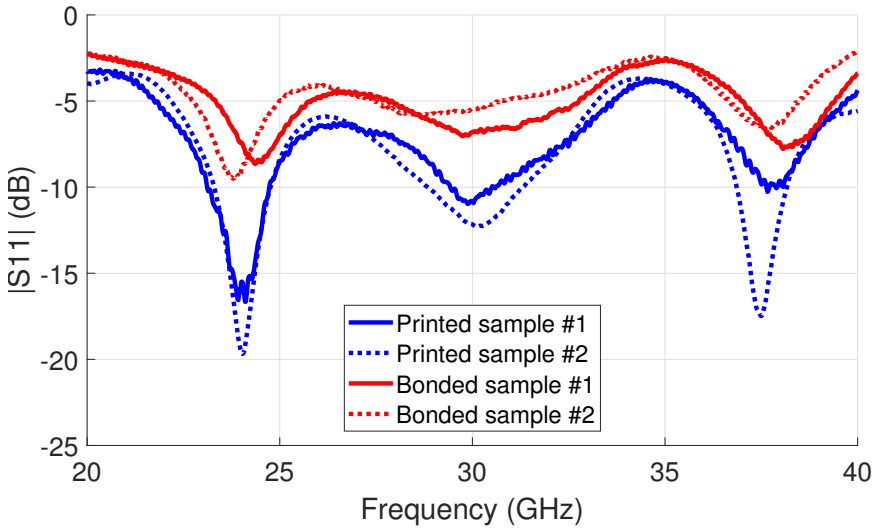


Figure 5.16: Measured S-parameters for cavity-embedded LNA MMIC with printed transitions and ribbon bonds demonstrates an improvement in S11 performance due to shorter bond length.

ALH369 die, a Ka-band LNA MMIC. Traditionally, MMIC devices require ribbon bonding for the RF interconnects, so it is necessary to offer a comparison between the traditional and the new technique. Fig. 5.15 shows perspective images of the bonded and printed transitions with the proof-of-concept LNA ICs. In order to evaluate this effectiveness, LNA evaluation boards were fabricated on a MEG6 laminate using an LPKF milling machine and manual chip placement process using an inkjet-printed SNP die attach. Two samples utilizing each technique were fabricated to ensure reliability and consistency. The gaps between the chip edge and the transmission lines were chosen to be $400\,\mu\mathrm{m}$ for two reasons. First, it allows extra space to prevent the printed die attach within the cavity from spreading up to the top layer circuity of the board, which can lead to short circuit of the transmission line. Additionally, it gives spacing for the ribbon bonding tool to make a good connection due to the size of the ultrasonic head. Optimally, shorter interconnects are better, but the ribbon bonds in this effort were kept at the lowest possible length due to these factors and are shorter in length than in others RF bonds found in other literature [79, 80, 81]. The ribbon bond interconnects have an average length of $550\,\mu\mathrm{m}$, width of $75\,\mu\mathrm{m}$, and average height of $132\,\mu\mathrm{m}$. The length of the bond wire increased due to the increase in bond height

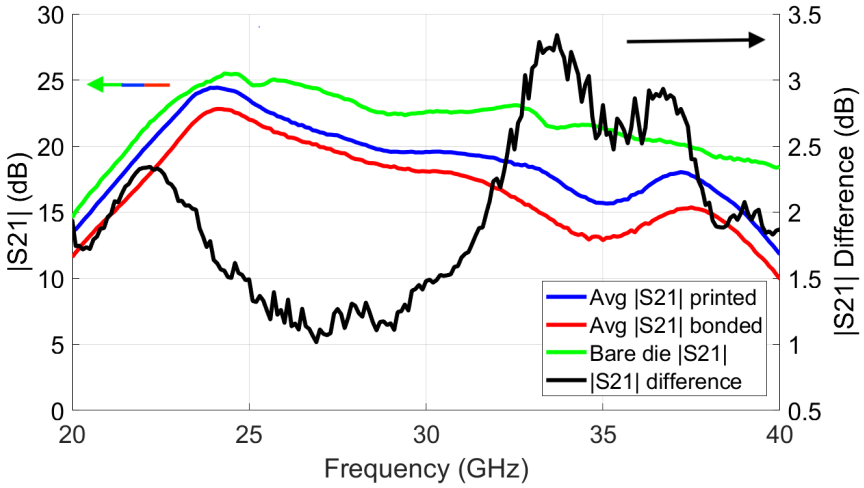


Figure 5.17: (Left axis) average insertion loss for printed and bonded samples. (Right axis) difference in insertion loss between printed and bonded samples (printed minus bonded). The bare die (without interconnects or evaluation board) measurement is shown in green as a reference.

and the additional wedge length required to create a mechanically and electrically solid connection.

The measured S-parameters for the printed and bonded transitions are shown in Fig. 5.16. Return loss measurements show a clear improvement in matching for the inkjet-printed transitions across the entire frequency range due to reduced interconnect length and profile height. Gain measurements show relatively similar trends for both printed and bonded transitions, where improvements are witnessed across the mesured frequency range. In an effort to better understand the effects of the proposed interconnects on amplifier gain, the $|S21|$ measurements of the two printed and two bonded interconnect devices are averaged accordingly and subtracted from one another to identify the difference in gain. Fig. 5.17 presents the average gain versus frequency of the LNA with printed and bonded transitions (left axis). The average $|S21|$ measurements for bonded transitions are subtracted from the average $|S21|$ of the printed transitions, yielding a plot of $|S21|$ difference presented in Fig. 5.17 (right axis). From the measurements, it is clear that due to the decreased interconnect length and inductance, better matching was achieved leading to a lower insertion loss or highger device gain performance. The average increase in the gain at least $1\,\mathrm{dB}$ and

with a peak of 3.3 dB improvement over the whole frequency range of 20–40 GHz. The improvement is especially noticeable in 30 GHz and above where the decreased inductance in the inkjet-printed interconnects translate to a weaker resonance.

5.3.3 Multi-Chip Module Front End Integration

With the demonstration of the inkjet-printed interconnects in a cavity-embedded assembly complete, fully functioning systems can utilize the inkjet printing technology for interconnection. For this effort a Ka-band MCM front end including LNA, PA, and RF switch is selected in order to multi-chip integration capabilities in a fully-printed assembly. The HMC-ALH369 LNA is used as the receiver amplifier, along with a Qorvo TGA4036 PA as the transmitter amplifier and a Qorvo TGS4302 switch as the switching module between the TX/RX and the shared output port, as shown in Fig. 5.18, allowing for time domain duplexing in a single module. All packaging and interconnection is done in a fully additive fashion utilizing the previously outlined processes. Instead of a copper circuit board interface, the entire circuit board conductor layer is inkjet printed on a bare Rogers 4003C laminate instead of MEG6 due to an improved degree of wetting and adhesion of the SNP ink on the Rogers substrate. This enhances the speed of production and demonstrates a reduction in the tooling required, as a major portion of the fabrication process is done entirely

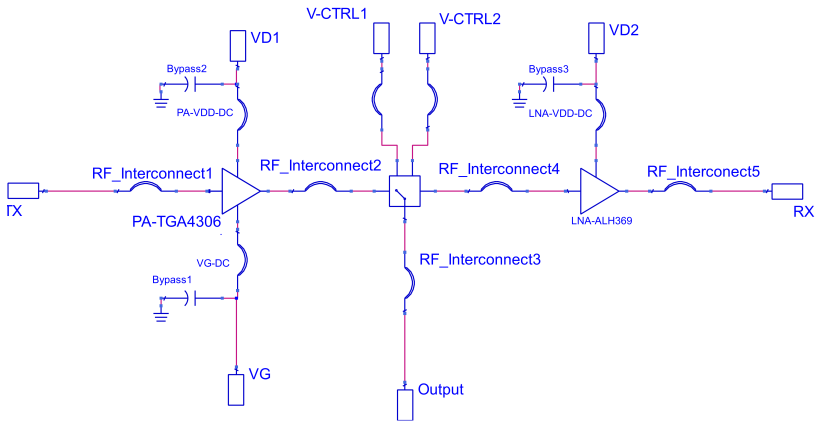
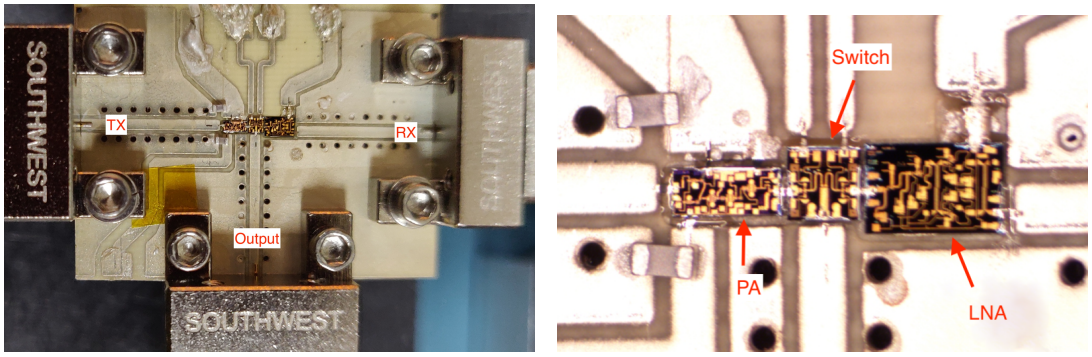
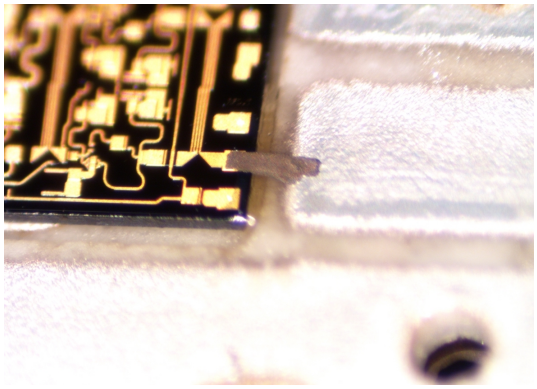


Figure 5.18: Schematic of the front end MCM, including LNA, PA, and RF switch ICs.



(a) (b)



(c)

Figure 5.19: Inkjet-printed mm-Wave front end MCM. (a) Full system interfaced with southwest end-launch connectors. (b) zoomed-in. (d) One of the inkjet printed RF interconnects on the output of the LNA.

on a single inkjet printer. The measured S-parameters of the MCM is plotted in Fig. 5.20, demonstrating the performance of both TX and RX chains, as well as the isolation between the TX and RX paths. From Fig. 5.20 the LNA and PA both turn on and provided gain, which is nominally around 3.5–$4\,\mathrm{dB}$ below the bare die measurements. This takes into account the losses of the switch MMIC and additional chip to chip (PA to switch, switch to LNA) interconnects and the transmission line losses and Southwest connectors, which is in line with the expected losses from this system.

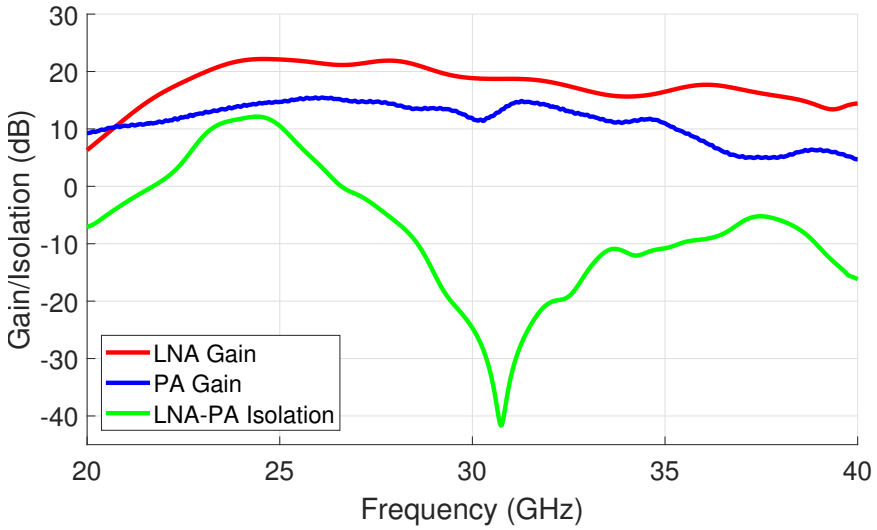


Figure 5.20: S-parameters of the front end module. Both LNA and PA |S21| are measured, along with isolation between the two when LNA and PA are both turned on. The resonance seen in the isolation is an inherent characteristic of the switch IC.

CHAPTER 6

3D/INKJET-PRINTED "SMART" PACKAGING FOR WIRELESS SIP

With the establishment of mm-Wave antenna and first-level interconnect integration utilizing inkjet printing techniques, focus is placed on the development of additive manufacturing processes to enable a new degree of 3D heterogeneous integration in the realm of wireless packaging. Specifically, the IC encapsulant is a feature of the wireless package with great potential for architectural expansion, where standard transfer molding procedures limit the degree of 3D integration and extended SiP functionality. Transitioning to an additive manufacturing approach incorporating a hybrid approach combining 2.5D inkjet printing and 3D printing promises an enabling divergence from the traditional laminate/encapsulant-based packaging schemes widespread throughout industry.

This chapter outlines the development and implementation of novel 3D-inkjet printing fabrication procedures to increase the versatility of the mm-wave MMIC package through 3D SiP integration and the realization of "smart" wireless packages. SLA 3D printing technology is targeted due to its collective benefits of high resolution, low surface roughness, and low equipment cost in comparison to other direct-write 3D printing technologies. This approach begins with the RF characterization of common SLA printing materials with the intent to determine relative permittivity (ε_r) and loss tangent (tan δ) within commercial mm-Wave operational bands, such as K_a- and E-band frequency ranges, for accurate high-frequency modeling and simulation. Further characterization of 3D-printed materials will evaluate parameters such as surface roughness and total surface free energy in order to determine compatibility with inkjet printing procedures. The convergence of these two technologies, inkjet and 3D printing, is prominent a goal of this research with the intent to demonstrate a highly versatile fabrication platform for the realization of "smart" wireless packages. The first-of-its-kind development of these "smart" packages involves the inte-

gration of fully-printed SiP components, such as 3D interconnects, antennas, passives, chip encapsulants, and shielding, all within a wireless mm-Wave module package. Additionally, sloped through-mold vias (TMVs) are presented as efficient interconnect solutions for 3D packaging architectures, enabling the development of highly-integrated SiP modules for wireless applications.

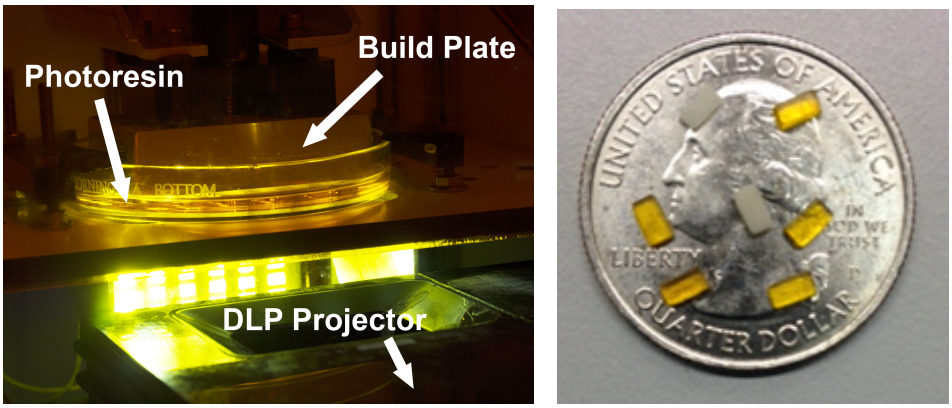
6.1 Hybrid 3D-Inkjet Printing for Advanced mm-Wave Packaging

The effectiveness of incorporating 3D printing with the presented inkjet printing packaging approaches requires the physical and electrical characterization of 3D-printed materials and their respective fabrication processes. This section outlines the RF characterization of 3D-printed SLA materials in the mm-Wave regime [64]. These materials are then demonstrated for use as arbitrarily-shaped IC encapsulants, fulfilling the traditional role of mechanical protection along with a newly acquired diversity in functionality for wireless packages. Additionally, surface roughness characteristics of 3D-printed structures are measured in order to assess printability in a hybrid 3D-inkjet printing approach [82].

6.1.1 3D-Printed Dielectric Characterization

The accurate dielectric characterization of these 3D-printed SLA materials is necessary in order to efficiently simulate and assemble mm-wave wireless systems in an additive and robust fashion. Waveguide fills with dimensions $3.01 \times 1.55 \times 1\,\mathrm{mm}$ are fabricated in order to fill $1\,\mathrm{mm}$ thick WR-12 waveguide spacer shims, as shown in Fig. 6.1. An Agilent N5242A PNA-X is used along with VDI WR12-VNAX frequency extenders to enable E-band measurements of the SLA dielectric samples.

Modeling methods satisfying the Kramers–Kronig relation are used to extract the relative permittivity and loss tangent of the printed materials from the measured S-parameters. Fig. 6.2. shows the extracted measurements of (a) relative permittivity and (b) loss tangent for the printed samples over the range of 55–$95\,\mathrm{GHz}$. Relative permittivity (ϵ_r) measure-



(a) (b)

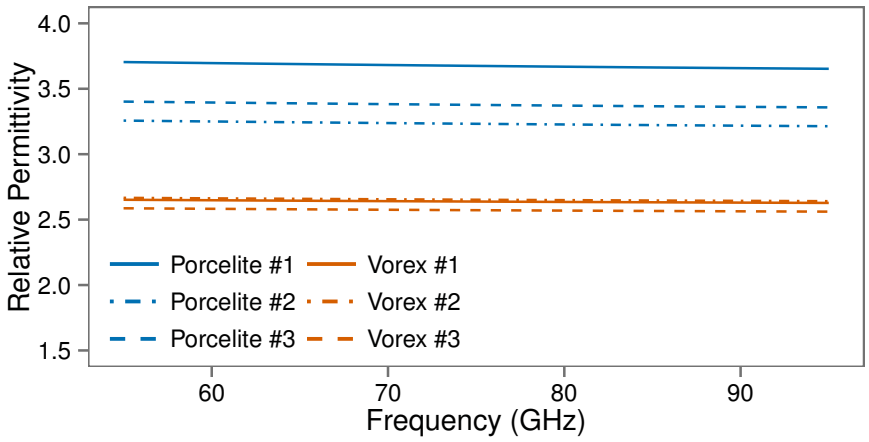
Figure 6.1: (a) Little RP 3D SLA printer setup, showing layer exposure with a DLP projector. (b) 3D-printed E-band waveguide fills for RF material characterization.

ments appear stable and fairly linear for frequencies up to above $90\,\mathrm{GHz}$ with a small downward slope as frequency increases. As expected, the ceramic-loaded Porcelite material exhibits a higher ϵ_r due to the presence of high-ϵ_r ceramic composites. The variation of the ϵ_r measurements for the Porcelite material are likely the result of dimensional variations for the waveguide fill samples due to the developing tuning of the processing conditions for this resin. Currently, relative permittivity measurement variations of less than $\pm 2\%$ and $\pm 7\%$ are achieved for the Vorex and Porcelite samples, respectively. Loss tangent ($\tan\,\delta$) measurements yield maximums of 0.019 and 0.026 for the Vorex and Porcelite samples, respectively, demonstrating their suitability for mm-wave RF applications.

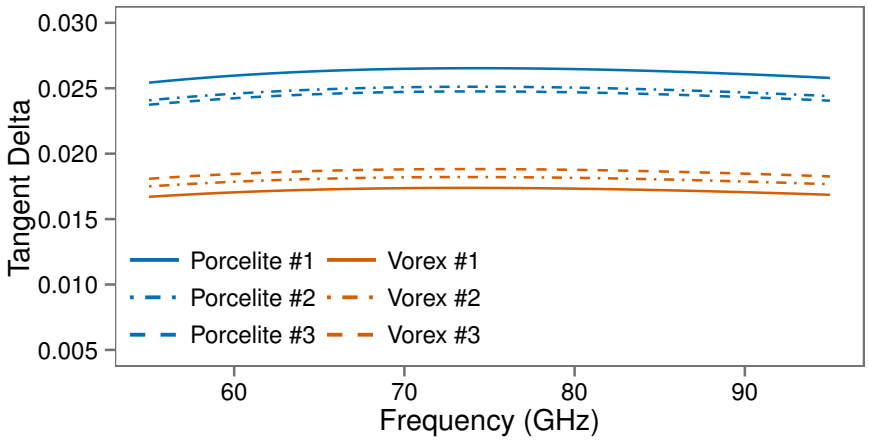
6.1.2 Arbitrarily-Shaped IC Encapsulants

The printing of an IC die encapsulation using the above SLA materials is presented with the goal of replacing standard epoxy molding and stamping methods of package encapsulation. In addition to being an ambient-pressure room-temperature fabrication process, SLA printing allows for the simple realization of selectively-patterned and nontraditionally-shaped encapsulation solutions, while simultaneously maintaining tan δ within the same range of standard epoxy molding compound materials [83].

Silicon dies with $280\,\mu\mathrm{m}$ thickness and areas of $2\times2\,\mathrm{mm}$ and $3\times3\,\mathrm{mm}$ are attached to



(a)



(b)

Figure 6.2: E-band characterization of (a) relative permittivity and (b) loss tangent for 3D-printed SLA materials extracted from S-parameters.

a metallic QFN leadframe using an inkjet-printed polymer-based ink. After the dies are attached, $5.5 \times 5.5 \times 1$ mm encapsulations are printed directly onto the dies using the Vorex and Porcelite materials and the outlined processing conditions. This is accomplished by affixing the QFN leadframes to the build plate of the SLA printer in order to directly pattern the die encapsulations onto the leadframes. Fig. 6.3 presents images of the printed Vorex and Procelite encapsulations. In addition to the standard encapsulation, an SLA printing tool can be configured to fabricate nontraditional encapsulation shapes, for example open cavities for microelectromechanical systems (MEMS) sensors and dielectric lenses for package-integrated antennas, presented in Fig. 6.3(c). These novel package shapes can

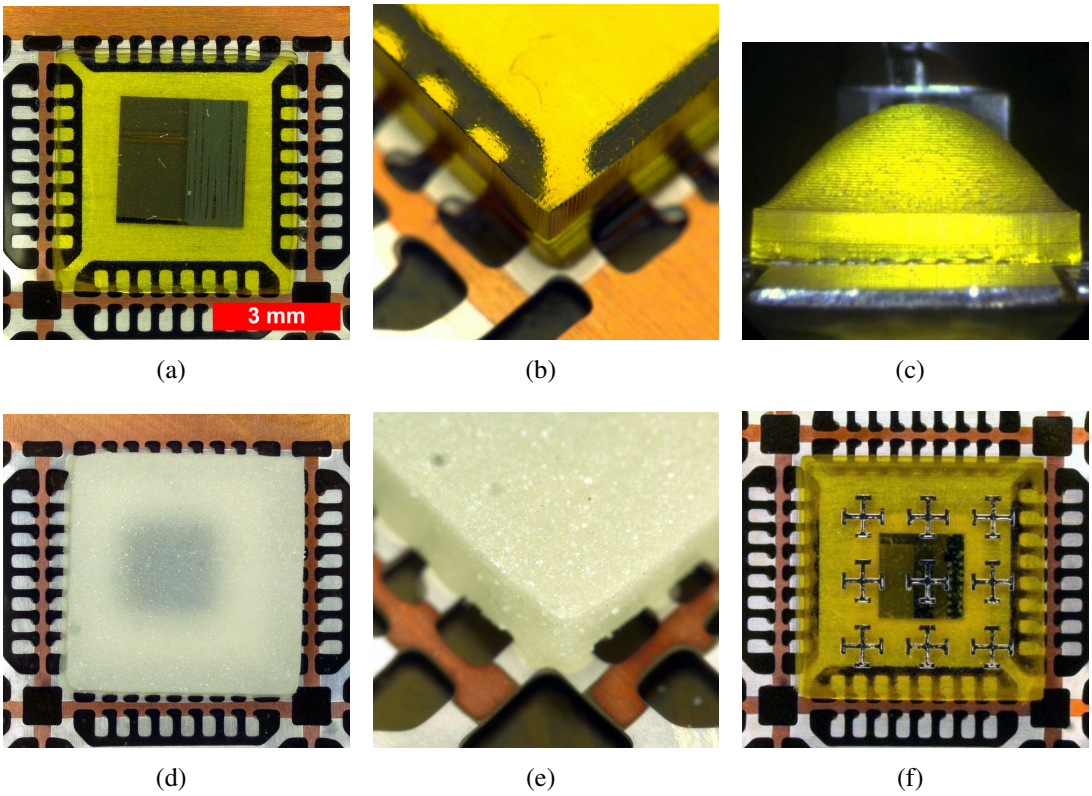


Figure 6.3: 3D-printed die encapsulations on a metallic QFN leadframe: Vorex encapsulation (a) top view and (b) perspective view, (c) Vorex dielectric lens structure; Porcelite encapsulation (d) top view and (e) perspective view; (f) Vorex encapsulation with inkjet-printed metamaterial.

be achieved by simply changing the 3D model in the SLA printing tool, highlighting the reconfigurable nature of this technology for diverse application-specific packaging applications.

6.1.3 Surface Roughness Assessment for Hybrid Printing

This newly demonstrated SLA printing technology for packaging can be easily combined with existing inkjet printing technology to realize the post-process fabrication of on-package components, including passive components, antennas, sensors, and metamaterial structures. The roughness of a 3D-printed SLA surface must first be investigated in order to ensure the efficient printability of post-process multilayer structures on top of a printed encapsulation. An Alpha-Step D-500 surface profilometer from KLA Tencor is used to mea-

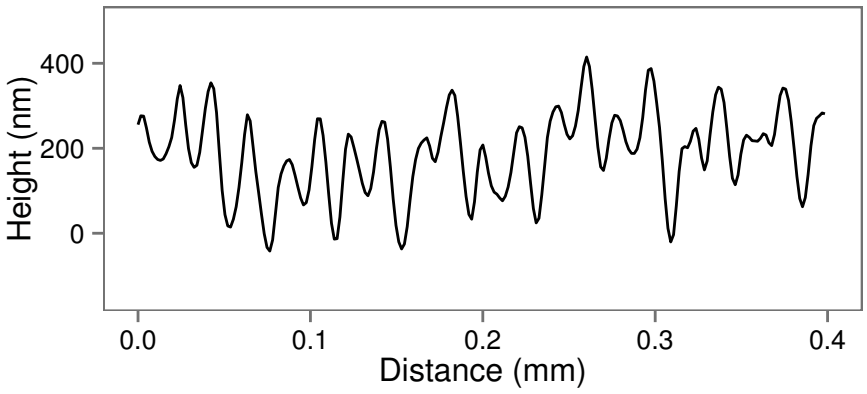


Figure 6.4: Profilometer measurement of a 3D-printed SLA encapsulation surface.

sure the surface of an SLA encapsulation. The surface measurements, shown in Fig. 6.4, exhibit a $\sim 40\,\mu\mathrm{m}$ periodicity that is to be expected from the width of the DLP projector pixels used to pattern each layer of the 3D print. The distance from the valley to the peak of each period is less than $400\,\mathrm{nm}$, a $25\times$ reduction compared to the minimum surface roughness typically achieved with standard fused deposition modeling (FDM) 3D printing technologies [30]. This drastic reduction in surface roughness allows for the post-process printing of metallic and dielectric topologies without the need for intermediary passivization films.

Fig. 6.3(f) presents a periodic frequency selective surface (FSS) inkjet-printed directly onto a 3D-printed encapsulation using a Dimatix DMP-2831 inkjet printing system and silver nanoparticle-based ink for such applications as wireless filtering and aperture coupling, which will be discussed further in Section 6.4.

6.2 Fully-Printed Through-Mold Via Interconnects

One of the most enabling features of utilizing additive printing technologies for microelectronic encapsulant design and fabrication is the concept of application-specific reconfigurability. Specifically for wireless packaging, industry standard epoxy mold compound (EMC)-based transfer molding techniques are limited to square encapsulants for the protec-

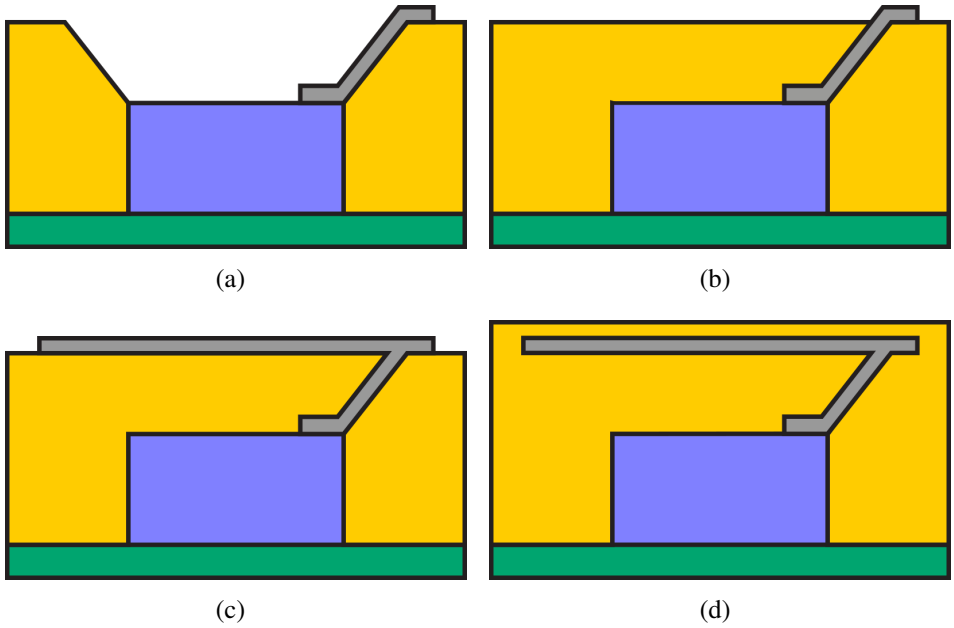


Figure 6.5: "Smart" wireless encapsulant process flow: (a) 3D print partial encapsulant (yellow) with die (violet) and inkjet print sloped TMV (grey) on a packaging substrate (green). (b) Cap partial encapsulant with photopolymer resin leaving exposed TMV interconnecting to embedded die. (c) Inkjet print antenna, passive, or other SiP component. (d) 3D print final encapsulant.

tion of the monolithic microwave integrated circuit (MMIC) die embedded within. However, through the development of arbitrarily-shaped encapsulants with 3D printing, functionality can be integrated into the microelectronic encapsulant in the form of antennas, passives, and other components to achieve on-demand, unique SiP solutions for a variety of wireless applications.

Through-mold vias (TMVs) are essential components for the development of 3D "smart" encapsulants for wireless device packages. Fig. 6.5 outlines the conceptual process flow for the fabrication of TMVs and SiP wireless encapsulants with 3D and inkjet printing [84]. Fabrication begins with the 3D printing of a partial IC encapsulant with sloped walls leading from the edge of the IC to the top of the encapsulant. TMV interconnects are then patterned with inkjet printing directly onto the pads of the IC, leading up the slope of the 3D-printed partial encapsulant to the top plane of the encapsulant. Next, 3D printing is used to seal the partial encapsulant, leaving the inkjet-printed interconnects exposed at the

new top plane of the encapsulant. Multilayer antenna array and/or passive components are then inkjet printed directly onto the encapsulant, interfacing with the TMVs leading up from the die. Finally, 3D printing is used to seal the wireless package. This combination of inkjet and 3D printing technologies enables the realization of highly-integrated 3D SiP designs in a low-cost, highly reconfigurable and scalable fashion to create intelligent wireless packages. The efforts outlined in this section are focused on the concepts presented in Fig. 6.5(a–b): printed ramped TMV fabrication and partial encapsulant capping.

6.2.1 Arbitrarily Sloped mm-Wave Interconnects for Printed SoP

With the ability to inkjet print electronic structures directly onto a 3D-printed encapsulation, interest is placed onto how these structures can interface with a molded IC within the package. The concept of directly interconnecting a molded IC die to an external plane of its encapsulation is an area not widely covered in literature. Amkor Technology Inc. (Chandler, AZ, USA) has demonstrated a through-mold-via (TMV) process for package-on-package (PoP) integration, however interconnects are limited to solder balls typically used with ball grid array (BGA) packages [85]. Due to the interest in SoP design solutions for mm-wave wireless systems, efficient TMV interconnects in the mm-wave regime are desired to expand the possibilities of system integration.

Before the inkjet printing of TMVs can take place, the roughness of the 3D-printed sloped sidewalls featured in the partial encapsulant test vehicle is investigated. An Alpha-Step D-500 surface profilometer from KLA Tencor is used to measure the stair-step discontinuities inherent with the SLA 3D printing technique. Fig. 6.6(a) presents the measured profile of the 3D-printed sloped sidewall using a $10\,\mu\mathrm{m}$ layer print height. The expected stair-step profile is apparent in the profilometer scan, where a step periodicity of approximately $40\,\mu\mathrm{m}$ is measured across the length of the $700\,\mu\mathrm{m}$-length ramps corresponding to the size of the pixels used with the DLP SLA 3D printer. In an effort to reduce the rough stair-step profile of the sloped sidewalls, SU-8 polymer ink is inkjet-printed across the par-

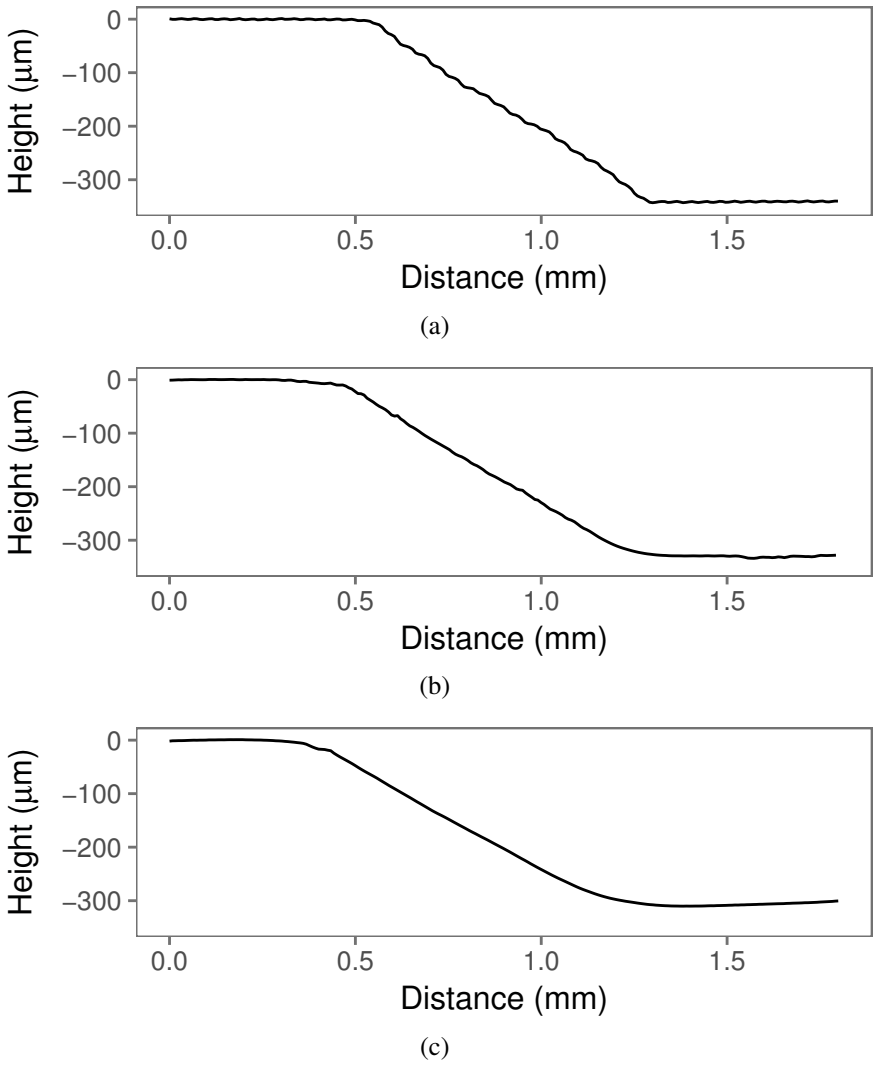
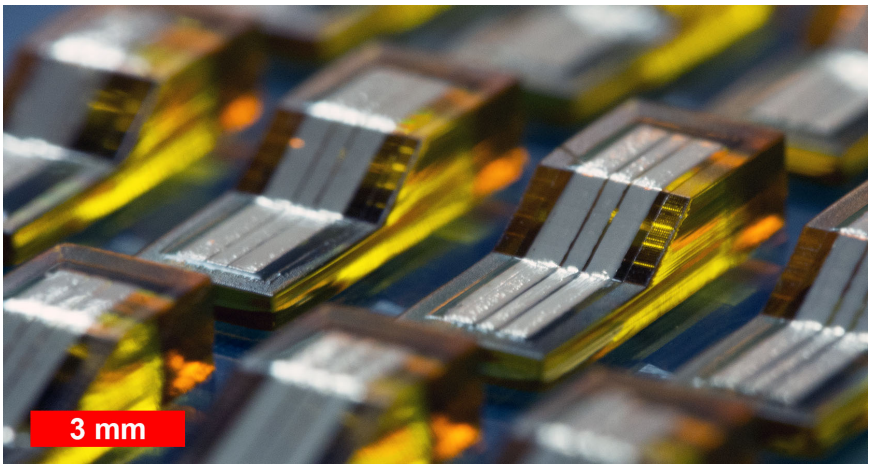
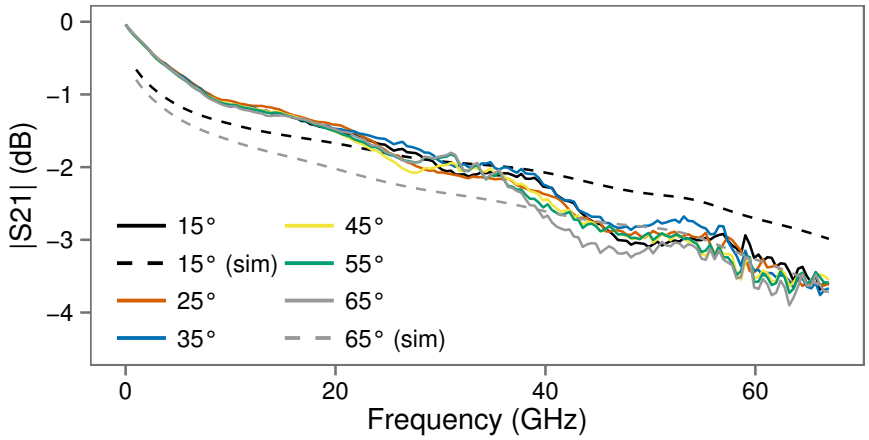


Figure 6.6: Surface profilometer scans of 3D-printed partial encapsulant sloped sidewalls with varying layers of printed SU-8 polymer passivation: (a) 0 layers, (b) 1 layer, (c) 2 layers.

tial encapsulant where the TMV interconnects will be subsequently printed. Fig. 6.6(b–c) present the measured surface profiles of the sidewalls with one and two printed layers with $20\,\mu\mathrm{m}$ drop spacing. With one layer of inkjet-printed SU-8 passivation, the stair-step profile of the sidewalls is greatly reduced leaving only several discontinuities. Additionally, two layers of SU-8 passivation essentially eliminate all stair-step discontinuities, leaving a smooth transition from the top to the bottom planes of the partial encapsulant. From these results, it is determined that two layers of inkjet-printed passivation is adequate for



(a)



(b)

Figure 6.7: (a) 3D-printed ramp structures with inkjet-printed CPW interconnects, highlighting the 35° slope ramps. (b) |S21| insertion loss measurements (—) and simulations (– –) of printed CPW TMVs with varying slope.

realizing a smooth sidewall profile within a partial encapsulant.

The integration of inkjet printing with 3D printing technology requires an analysis of the capabilities of this typically 2/2.5D technology in truly 3D applications. In order to evaluate SLA 3D printing technology for integration with inkjet printing for mm-wave packaging, ramped interconnect structures with slopes ranging from 15–75° are characterized with the Vorex SLA material. Sample Vorex ramps measuring $3\times7.5\,\mathrm{mm}$ with a $1\,\mathrm{mm}$ tall ramp and $10\,\mu\mathrm{m}$ layer height resolution are fabricated with the LittleRP SLA printer to represent the sloped walls of an IC encapsulation. Next, two layers of a MicroChem SU-

8 polymer-based ink are printed onto the ramp structure in order to passivate the $10\,\mu\mathrm{m}$ layer steps of the 3D-printed ramps with a film thickness of approximately 8–$12\,\mu\mathrm{m}$. Sun Chemical EMD5730 silver nanoparticle-based ink is printed to pattern coplanar waveguide (CPW) interconnect lines from the die-level to the encapsulation-level of the ramp structures. Finally, the printed ramp interconnects are sintered in an oven at $150\,^{\circ}\mathrm{C}$ for 1 hr to complete the fabrication process. Fig. 6.7(a) shows a perspective micrograph of the test vehicle containing multiple samples of the SLA ramps with varying slope. |S21| insertion loss of the printed TMV interconnects is characterized up to $67\,\mathrm{GHz}$ with an Agilent E8361C PNA and 67A-GSG-250-C probes from GGB, presented in Fig. 6.7(b) along with simulations for the two extreme cases (15° and 65°). All slopes ranging from 15–65° exhibit an insertion loss between 0.5–$0.6\,\mathrm{dB/mm}$ at 60 GHz, where the 75° slope did not achieve complete electrical connectivity. The printed 3D interconnects presented in this paper yield a $7\times$ reduction in insertion loss from standard wirebond interconnects at $60\,\mathrm{GHz}$ [49].

6.2.2 Partial Encapsulation Process with Through Mold Vias

To evaluate the feasibility of integrating TMV interconnects within a microelectronic encapsulant using additive printing technologies, a 3D test vehicle is designed featuring a partial encapsulant with sloped sidewalls. The sloped sidewalls bridge the top of the encapsulant to the bottom plane of the cavity $400\,\mu\mathrm{m}$ below with an angle of 30°. 3D printing fabrication of the test vehicle is performed on a glass carrier utilizing a $10\,\mu\mathrm{m}$ layer print height in order to reduce the discontinuous step height of the sloped sidewalls of the design. Fig. 6.8(a) presents a micrograph of the 3D-printed partial encapsulant test vehicle.

Fig. 6.8(b) and (d) present micrographs of the fabricated inkjet-printed TMVs on the 3D-printed partial encapsulant test vehicle. Following the inkjet-printing of the sloped TMVs, the partial encapsulant is then capped through the syringe deposition of Vorex photopolymer resin within the encapsulant cavity. Finally, the capped encapsulant undergoes a $3\,\mathrm{J/cm^2}$ UV exposure and wash with IPA and deionized water. Micrographs of the fully-

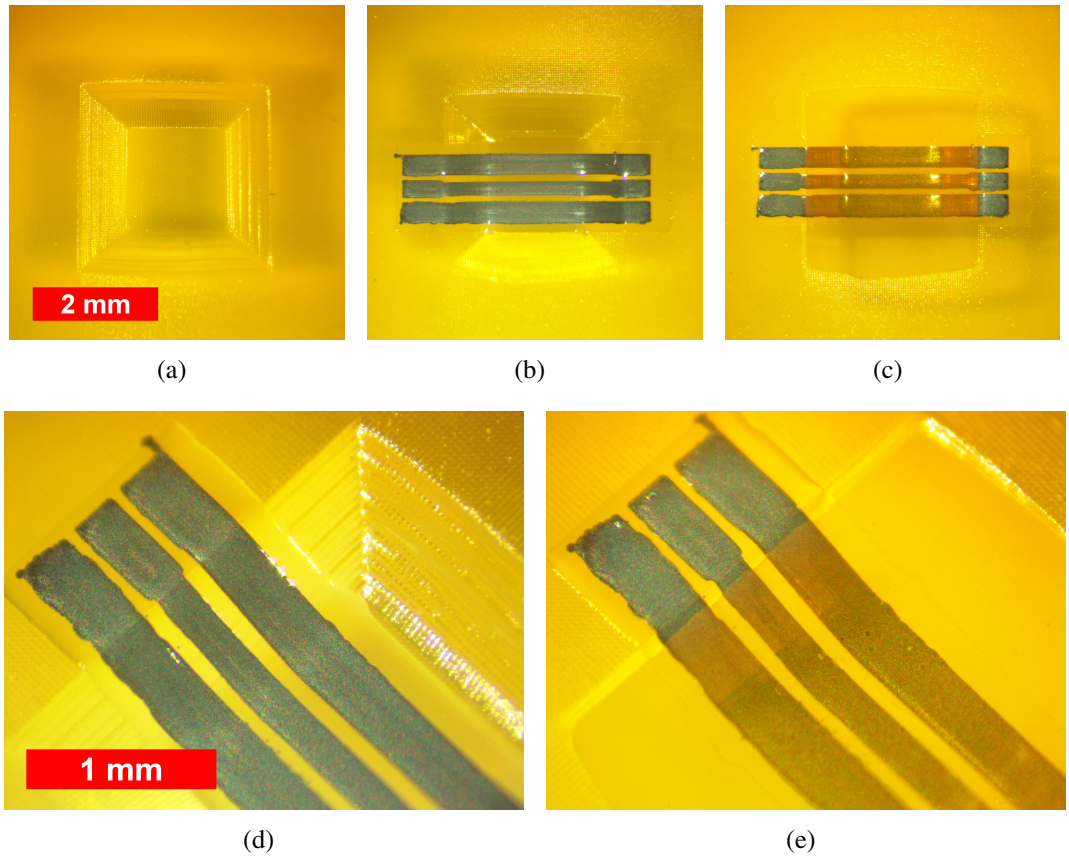
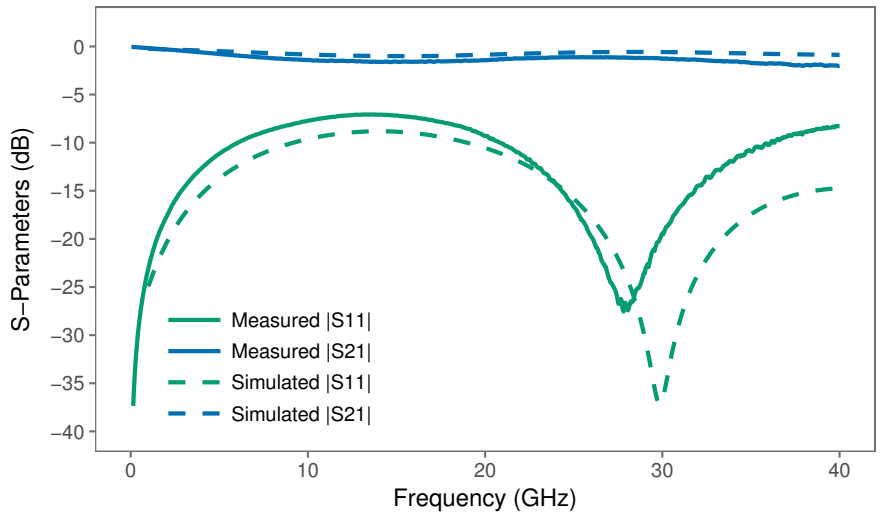


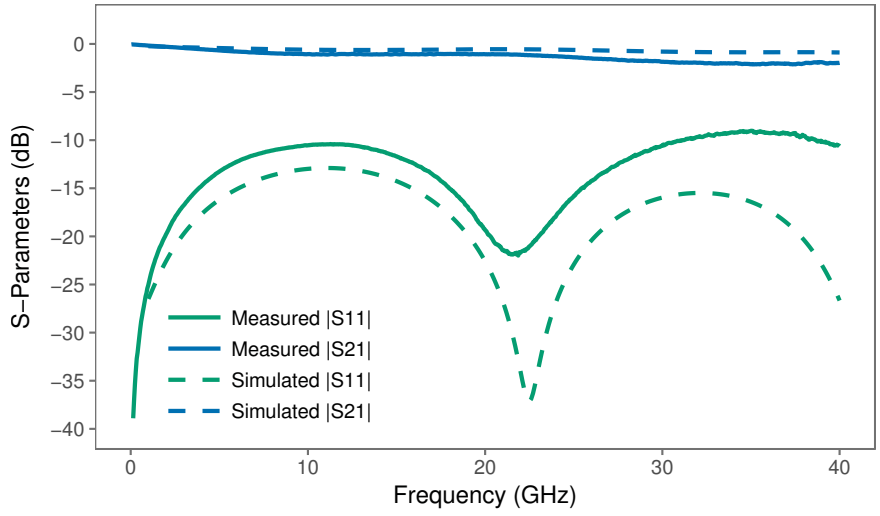
Figure 6.8: 3D-printed test vehicle for inkjet-printed TMV and partial encapsulant capping verification: (a) 3D-printed partial encapsulant, (b) inkjet-printed TMVs and (d) perspective detail, (c) capped TMV-integrated encapsulant and (e) perspective detail.

printed and capped TMV interconnects are presented in Fig. 6.8(c) and (e).

The S-parameters of the inkjet/3D-printed TMVs are measured from 10–40 GHz using an Anritsu 37369A VNA with Cascade Microtech ACP40-GSG-250 probes. Simulated and measured return and insertion loss are plotted in Fig. 6.9 for both partial encapsulant and capped printed TMVs. The return loss measurements exhibit improved matching for the capped samples, where maximum $|S11|$ is measured to be -7.1 dB at 13.8 GHz for the partial encapsulant and -9.1 dB at 34.5 GHz for the capped encapsulant. Furthermore, the resonances present in the return loss measurements experience a shift from 27.8 GHz to 21.5 GHz due to the dielectric loading of the capping dielectric above the CPW line within the encapsulant. Insertion loss is measured to be 2 dB for both samples at 40 GHz,



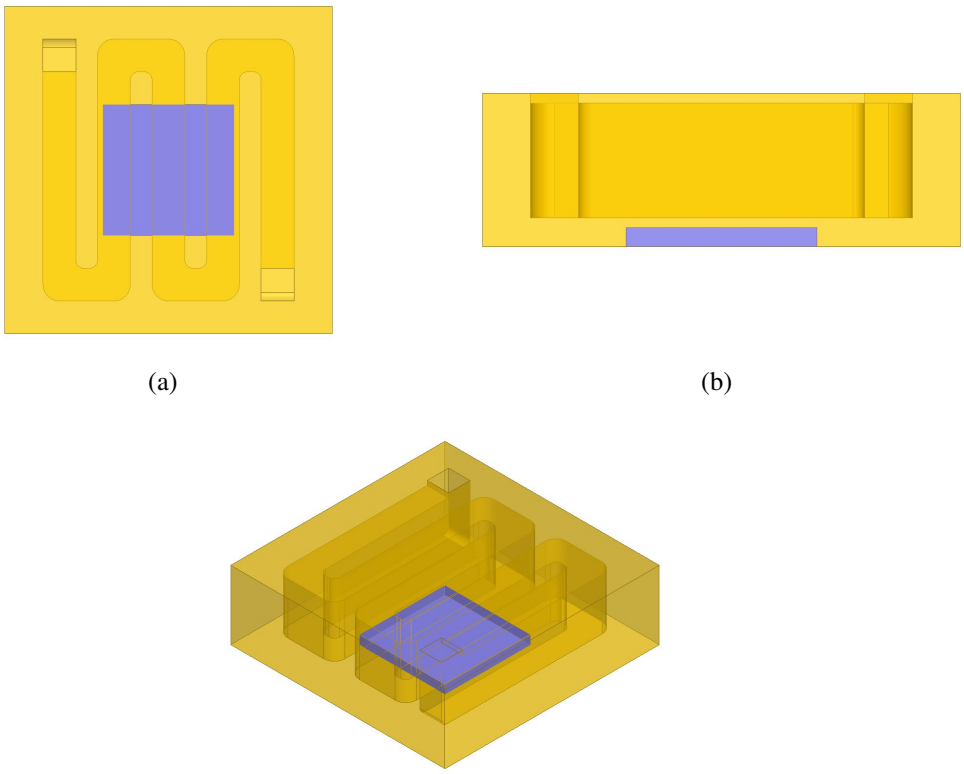
(a)



(b)

Figure 6.9: S-parameter measurements of simulated and fabricated inkjet/3D-printed TMVs (a) before and (b) after capping of the partial encapsulation.

yielding a line loss of $0.46\,\mathrm{dB/mm}$ at $40\,\mathrm{GHz}$ for the $4.3\,\mathrm{mm}$-length CPW line. Deviations between the experimental and simulated measurements are present for both sample topologies and are likely to be improved through the continued characterization of SLA photopolymers materials at Ka-band (26.5–$40\,\mathrm{GHz}$), where parameters of loss tangent and relative permittivity of the Vorex material were extrapolated from E-band (60–$90\,\mathrm{GHz}$) characterization data for this effort [64]. Overall, the results of both of the fully-printed partially-encapsulated and capped TMV interconnects demonstrate the effectiveness of the



(a) (b)

(c)

Figure 6.10: CAD model of 3D-printed microfluidic-integrated encapsulant with silicon die: (a) top, (b) side, and (c) perspective views.

technology for the fabrication of 3D package-integrated interconnects for wireless SiP applications.

6.3 Package-Integrated Microfluidic Channels

As a maskless and moldless technology, 3D printing enables the design of arbitrarily-shaped and integrated microelectronic encapsulants with embedded IC dies. One such example of the capabilities of the technology for this application is the integration of microfluidic channels directly within an IC encapsulant [84]. Package-integrated microfluidic channels can serve several purposes, including fluid-controlled circuit tuning, fluid component sensing, and liquid cooling for thermal management.

As a proof of concept demonstration, a 3D-printed microlfluidic-integrated encapsu-

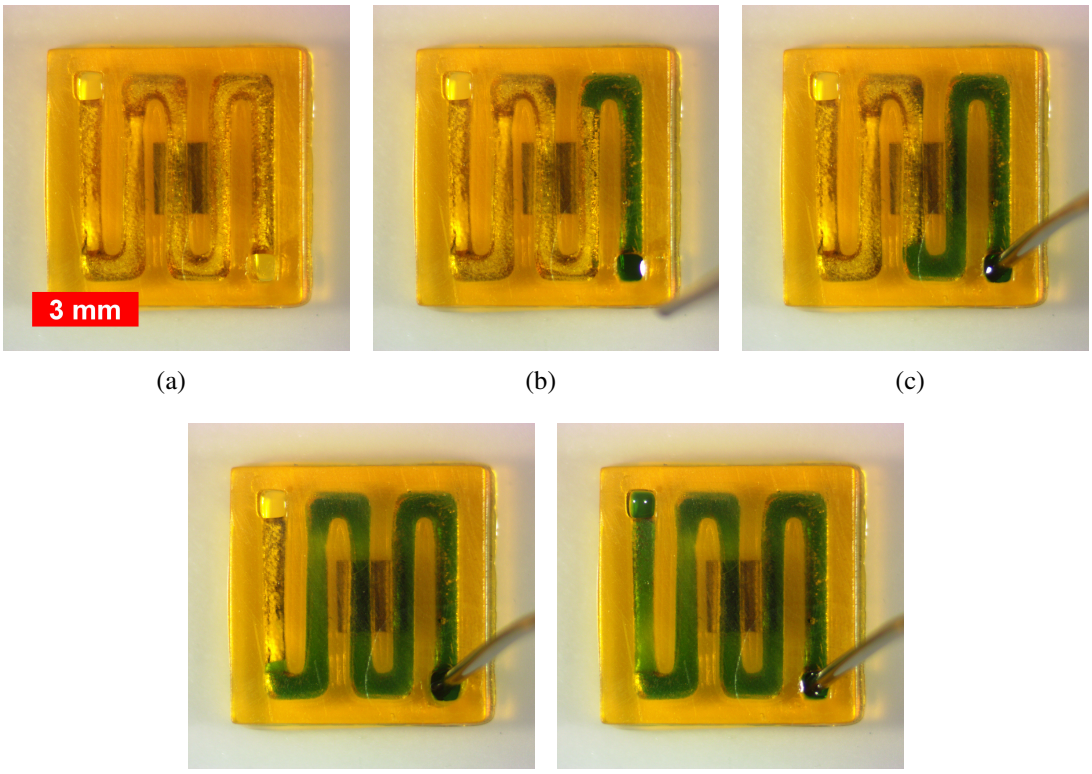


Figure 6.11: 3D-printed microfluidic-integrated encapsulant with silicon die: (a) empty channel, (b–d) partially filled channel, and (e) completely filled channel.

lant is designed for package-integrated thermal management. Fig. 6.10 presents a 3D microfluidic encapsulant model, featuring an inlet, outlet, and meandering channel atop the embedded die. The dimensions of the channel are designed to be $1.2{\times}0.5\,\mathrm{mm}$, yielding a full channel volume of approximately $12.8\,\mu\mathrm{L}$. The $5 \times 5{\times}1.4\,\mathrm{mm}$ encapsulant features a $100\,\mu\mathrm{m}$-thick passivation between the embedded die and the microfluidic channel, however could be removed allowing for the fluid channel to interface directly with the die if desired.

Fabrication of the microfluidic-integrated encapsulant begins with the same die attach and glass carrier process outlined in the previous section. Printing and post-print cleaning take place with the addition of three cleaning steps to remove photopolymer resin from the microfluidic channels before the final UV curing. First, compressed air is directed to the inlet of the microfluidic channel to expel the uncured resin within the channels. Next, IPA is loaded into the channel followed by a submersion and sonication in IPA for $5\,\mathrm{min}$. With

all uncured resin expelled from the channel, the post-print UV cure takes place to complete the fabrication process.

A micrograph of a 3D-printed microfluidic-integrated encapsulant with silicon die is presented in Fig. 6.11(a). In order to validate the post-print channel cleaning process and verify the integrity of the channel, the 3D-printed encapsulant is loaded with water dyed with blue food coloring. Fig. 6.11(b–d) present the fluid loading process using a syringe directly inserted into the channel inlet. From the micrograph in Fig. 6.11(d), it is apparent that the microfluidic channel is successfully voided of photopolymer resin after printing and that overcuring leading to channel blockage is not an issue.

6.4 Frequency-Selective Shielding and Polarizing Structures

As the density of wireless SiP modules increases, greater attention must be paid to the potential of system degradation from spurious radiation and electromagnetic interference (EMI). In order to address these detrimental phenomena, shielding structures may be employed through the integration of metallic lids and high-loss dielectric encapsulants [86]. However, the ability to selectively pattern frequency-selective shielding structures gives the advantage of blocking certain known interference bands while allowing for transparency in certain band of interest, which is especially advantageous for SiP architectures incorporating in-package antennas. This section outlines the development of 3D/inkjet-printed shielding structures using frequency selective surfaces (FSS) to enable robust shielding at the encapsulant level [84]. Additionally, inkjet-printed THz polarizers are presented to highlight the effectiveness of these additive manufacturing technologies beyond current mm-Wave centric implementations [87].

6.4.1 Encapsulant-Integrated mm-Wave Shielding

A cross-shaped slot FSS is designed to behave as a bandpass filter centered at 77 GHz. This design is the inverse of a common cross-shaped FSS which behaves as a bandstop

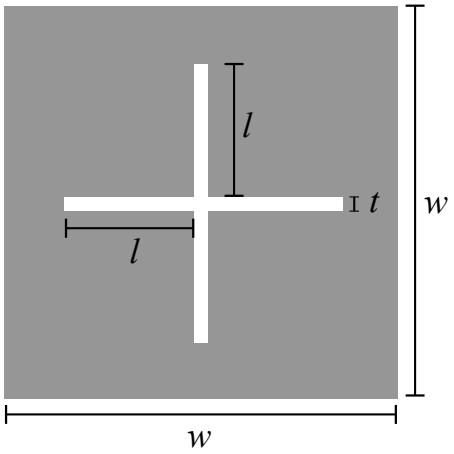


Figure 6.12: (a) Unit cell for periodic cross-shaped slot FSS designed for $77\,\mathrm{GHz}$ with dimensions: w = $1.9\,\mathrm{mm}$, l = $1.4\,\mathrm{mm}$, and t = $0.1\,\mathrm{mm}$.

filter [88]. Whereas a bandstop filter is useful for certain applications, a bandpass design is desired to highlight the post-process filtering and tunability of FSS-integrated wireless packages depending on their required application. Because the FSS will be present directly on top of the encapsulation of a wireless IC, the inclusion of the 3D-printed material is necessary for accurate modeling simulation. The 3D-printed material, discussed in the following section, has been characterized at $77\,\mathrm{GHz}$ through an E-band waveguide fill method and demonstrates the following electrical characteristics at $77\,\mathrm{GHz}$: ϵ_r = 2.6 and tan δ = 0.017. The 2D topology and dimensions of the FSS unit cell atop a 1 mm thick 3D-printed dielectric are presented in Fig. 6.12.

Simulations of the FSS unit cell are performed in HFSS using master-slave boundary conditions and Floquet port excitation. Insertion and return loss characteristics across the frequency range of 60–$90\,\mathrm{GHz}$ are shown in Fig. 6.13. The simulated S-parameters demonstrate a pass-band insertion loss of $-1.22\,\mathrm{dB}$ at the target $77\,\mathrm{GHz}$ with minimal return loss.

Encapsulant samples are printed using a custom LittleRP SLA 3D printer with a Viewsonic PJD7820HD DLP projector. The acrylate-based Vorex (orange color) photopolymer resin from MadeSolid is printed with $50\,\mu\mathrm{m}$ thick layers and an exposure time of $7\,\mathrm{s}$ to cure each layer. After the printing is complete, the samples are submerged in two baths of

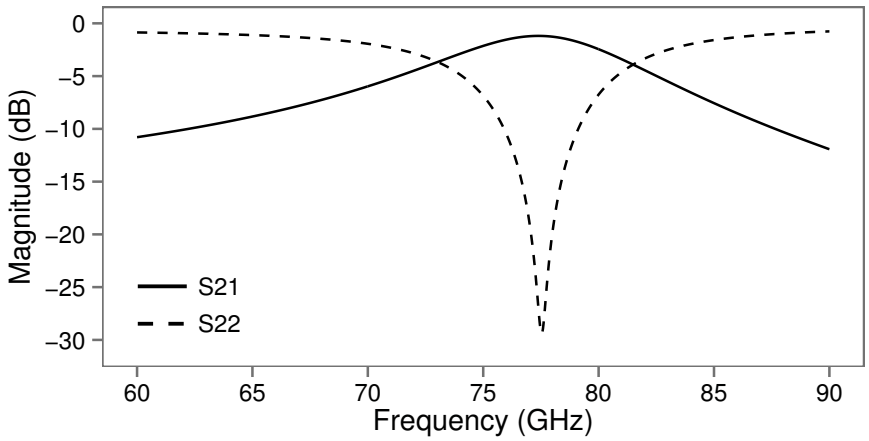


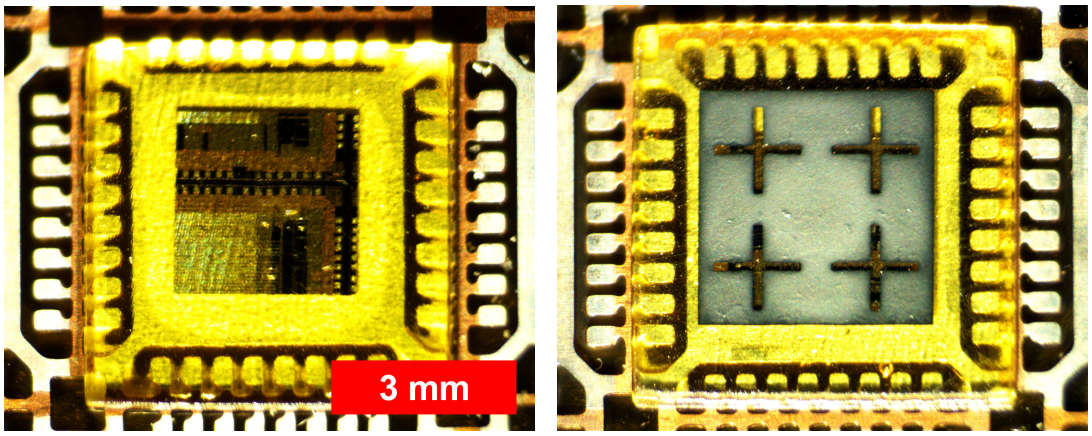
Figure 6.13: S-parameter simulations of cross-shaped slot FSS unit cell.

isopropyl alcohol to remove any excess resin. Finally, the 3D-printed samples are given a post-print $1\,\mathrm{J/cm^2}$ UV exposure to complete the fabrication process. Next, EMD5730 silver nanoparticle-based ink from Sun Chemical is printed to pattern the cross-shaped slot FSS designed to function as a bandpass filter centered at $77\,\mathrm{GHz}$. The proof-of-concept FSS topology is presented in Fig. 6.14(b) along with a bare 3D-printed SLA encapsulation in Fig. 6.14(a) for visual comparison.

6.4.2 Wire Grid Terahertz Polarizer

In the field of terahertz spectroscopy, polarized electromagnetic radiation enables the isolation and characterization of certain material properties through transmission and reflection measurements. Polarizers are crucial optical components, where the accuracy of spectroscopy measurements can depend directly on the degree of polarization. In the THz range, polarizers can be assembled in a wire-grid fashion, which are typically achieved using tungsten wire with a relatively high manufacturing cost. Additionally, high degrees of polarization often require the stacking of multiple polarizers which can further increase costs and limit practical measurement capabilities.

This effort presents for the first time the use of inkjet printing to realize THz polarizer structures with a dramatic decrease in manufacturing costs [87]. Wire grid polarizers are



(a) (b)

Figure 6.14: Proof-of-concept 3D-printed SLA encapsulations for wireless IC packaging: (a) bare encapsulation and (b) inkjet-printed FSS-integrated encapsulation.

printed on $5\,\mathrm{mil}$ Kapton 500HN films using the Sun Chemical EMD5730 SNP ink and sintered at $200\,^{\circ}\mathrm{C}$ for $2\,\mathrm{h}$, shown in Fig. 6.15. Numerous samples are printed with varying physical dimensions, including: the spacing between silver lines (G), the width of the lines (W), and the number of passes with the printer, or printed layers (L). Though this demonstration focuses on a laminate-based implementation, the inkjet printing process has the potential to apply the low-cost realization of THz polarizers at the package level to wireless module encapsulants in a fashion similar to the efforts presented in the previous section.

Samples are measured using time domain terahertz spectroscopy (TDTS) utilizing the excitation of photoconductive antennas called "Auston" switches with infrared femtosecond laser pulses. The figure of merit for these measurements is the degree of polarization (DoP), which is defined in Eq. 6.1 using the transmission of the polarizer when printed lines are aligned (T_{pass}) and perpendicular ($T_{polarize}$) to the incoming THz radiation.

$$DoP = \frac{T_{pass} - T_{polarize}}{T_{pass} + T_{polarize}} \tag{6.1}$$

The measured DoP for the printed polarizer samples are shown in Fig. 6.16, including

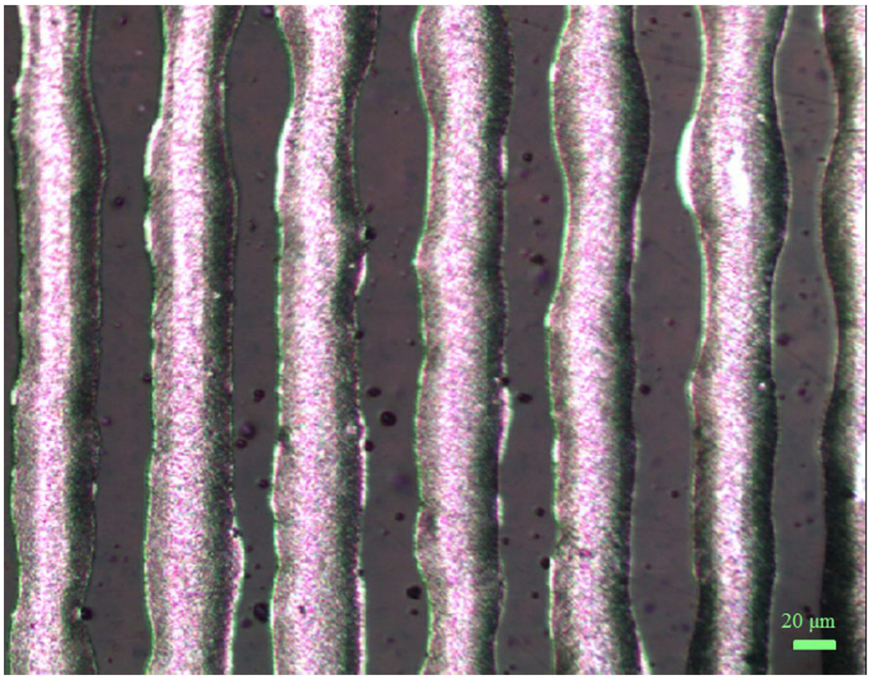


Figure 6.15: Inkjet-printed THz polarizer micrograph with $40\,\mu\mathrm{m}$ gap, $40\,\mu\mathrm{m}$ width, and 4 printed layers (40G/40W/4L).

variations in width, length, and printed layer count. Additionally, the red curve is measured using a stacked configuration with two 40G/40W/4L polarizers. The measurements show a trend where decreasing trace width and trace gap while increasing layer count results in increasing the quality of polarization. Additionally, the DoP of the stacked 40G/40W/4L polarizers is nearly identical to $1-(1-DoP)^2$ using the DoP of a single 40G/40W/4L polarizer, thus indicating that the stacked polarizers effectively behave as a series of independent polarizers. The stacked configuration of these polarizers is shown to be highly effective and comparable to commercial solutions in the 0.3–$1\,\mathrm{THz}$ frequency range. Further reduction in the gap size has the potential to increase the DoP, providing a competitive low-cost alternative to traditional wire grid THz polarizers with the highlighted capability of SiP integration for next-generation wireless systems.

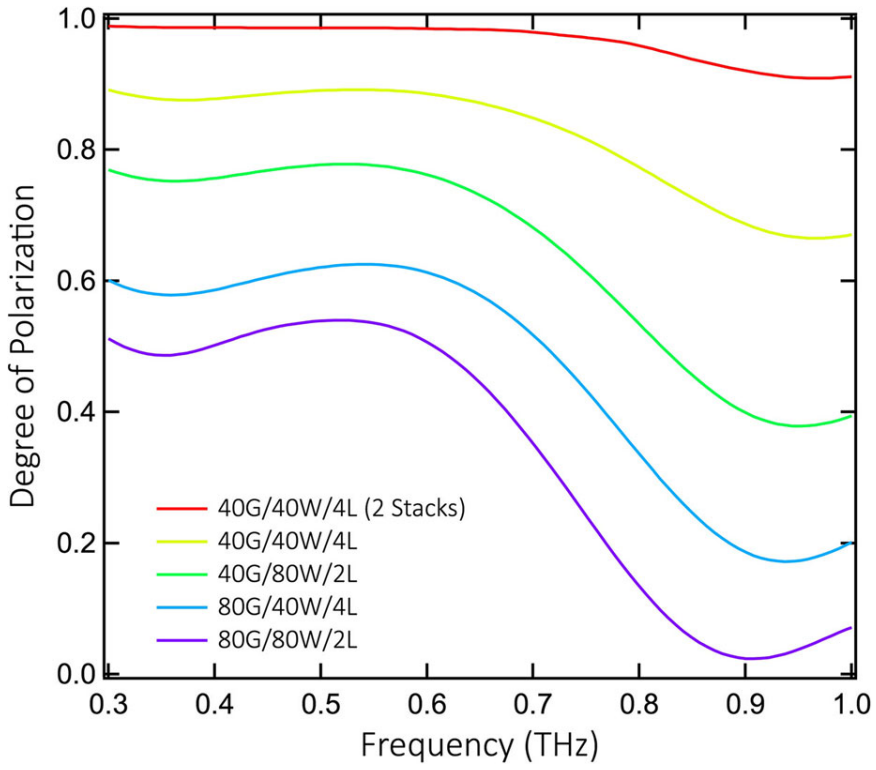


Figure 6.16: Measured degree of polarization (DoP) of inkjet-printed THz polarizers.

CHAPTER 7
CONCLUSIONS

The work presented in this dissertation outlines the development and implementation of advanced additive manufacturing techniques to expand upon the traditional design concepts and integration capabilities of wireless mm-Wave packaging architectures. Additive inkjet and 3D printing manufacturing procedures are presented and characterized for the development of high-gain mm-Wave antennas for SiP integration. The key enabling feature of this development is the ability to additively pattern multiple materials in a multilayer post-processing fashion, where RF substrates can be deposited on virtually any host or substrate. Fully-printed first-level interconnection methodologies are demonstrated for the first time and compared with traditional bonding techniques to yield improvements in both matching and insertion loss across the Ka-band with active MMIC devices. This is enabled through the conformal nature of inkjet printing in order to achieve a reduction of interconnect length and height in comparison with traditional techniques. Finally, the novel concept of "smart" wireless packaging is detailed with fundamental SiP component demonstrations utilizing a hybrid 3D-inkjet printing approach. The realization of arbitrarily-shaped IC encapsulants incorporating TMV interconnects, microfluidic networks, and frequency-selective shielding structures reaching into the THz regime further highlight the robust capabilities of heterogenous integration for wireless SiP design schemes enabled through additive manufacturing.

7.1 Contributions

The specific contributions of this dissertation are as follows:

1. mm-Wave Antenna Integration

(a) Process and material characterization for fully-printed RF substrates, including thick-film dielectric printing techniques, and RF material characterization through printed T-resonator and microstrip lines.

(b) Design and characterization of high gain mutlilayer $24.5\,\mathrm{GHz}$ proximity-coupled patch and Yagi-Uda antenna arrays utilizing printed dielectric substrates.

(c) Demonstration of fully-printed $30\,\mathrm{GHz}$ patch antenna integrated directly onto an IC molding.

2. Fully-Printed First-Level Interconnects for MMIC Devices

(a) Development of conformal multi-material inkjet printing processes to realize 3D interconnects for bare die MMIC devices.

(b) SiP integration of $30\,\mathrm{GHz}$ bow-tie antenna with fully-printed interconnection.

(c) Demonstration of fully-printed interconnects with Ka-band MMIC devices in surface mount assembly, including attenuator and LNA dies.

(d) Development of inkjet-printed gap-fill and interconnection process for cavity-embedded MMIC devices, yielding improved matching and gain improvements of up to $3.3\,\mathrm{dB}$ across Ka-band compared with traditional techniques.

(e) Fully-printed routing and interconnection for Ka-band MCM, including LNA, PA, and RF switch MMIC devices.

3. 3D/Inkjet-Printed "Smart" Packaging for Wireless SiP

(a) Development of hybrid 3D-inkjet inkjet printing approach, combining SLA 3D printing with inkjet printed passivation and conductive material patterning.

(b) E-band characterization and surface roughness analysis of 3D-printed SLA photopolymer resins.

(c) Demonstration of arbitrarily-shaped IC encapsulants for application-specific packaging.

(d) Development of fully-printed low-loss TMV interconnects for realizing 3D SiP architectures.

(e) Demonstration of functional "smart" encapsulant structures, including microfluidic networks, frequency-selective shields, and THz polarizers.

7.2 Future Efforts

The goal of this body of work is to present a foundation for the integration of additive manufacturing techniques within the design and manufacturing of mm-Wave wireless package architectures. The extension of this work involves the refinement of these fabrication procedures along with the further advancement of the tools and materials involved throughout. The maturation of commercially available conductive inks will provide great benefits to the reliability and yield of inkjet-printed components. Additionally, the development of low-loss dielectric materials for both inkjet and 3D printing has the potential to improve the electrical characteristics of fully-printed RF structures to meet or exceed those of traditional RF laminate materials. Though inkjet printing technologies have been steadily gaining maturity over the past few decades in the development of materials and tools for electronic fabrication, there is still great room for improvement with respect to 3D printing technologies, where focus is just beginning to branch out from the naturally prioritized mechanical considerations of printed structures in most commercial applications.

Finally, the hybrid inkjet and 3D printing approaches presented in this thesis are an attempt to break the mold of traditional electronic assembly and packaging schemes. In the realm of RF engineering, it can be challenging to consider 3D integration beyond typical 2.5D approaches involving multilayer laminate stacks, embedded chips, and canonical transmission line structures. The continued pursuit of novel 3D architectures require creativity in both design and implementation, for which additive manufacturing has continually proven to inspire.

7.3 Author's Publications

7.3.1 Journals

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